ARM High Performance Computing

ARM

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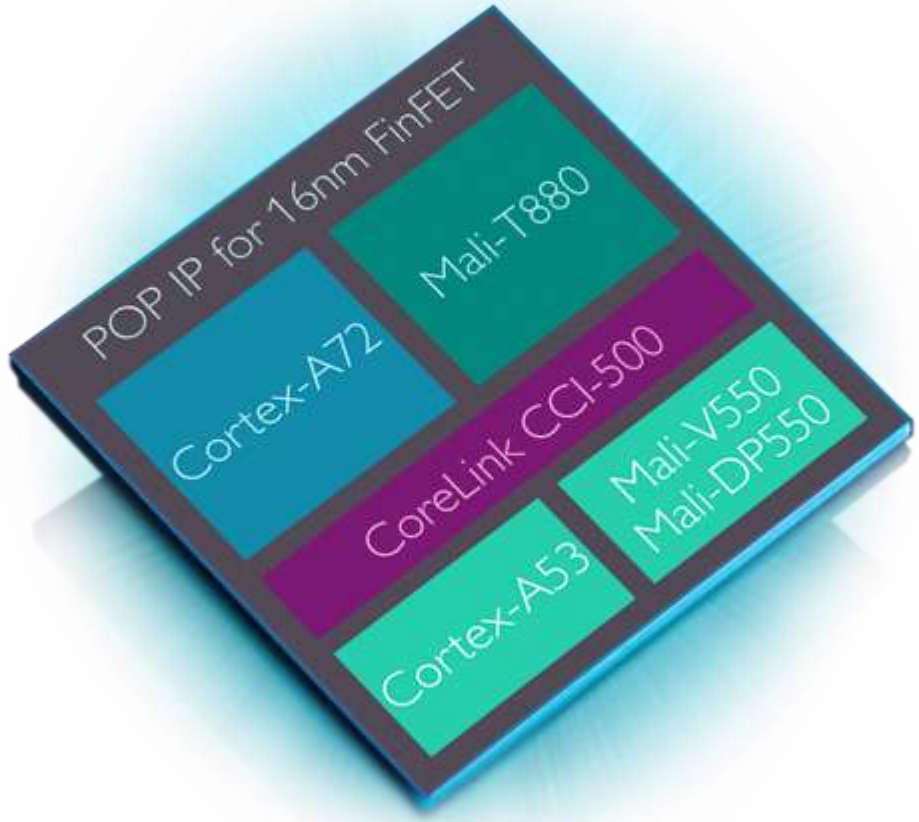
An introduction to ARM

ARM is the world's leading semiconductor intellectual property supplier.

We license to over 440 partners, are present in 95% of smart phones, 80% of digital cameras, 35% of all electronic devices, and a total of 72 billion ARM cores have been shipped since 1990.

Our CPU business model:

- License technology to partners, who use it to create their own system-on-chip (SoC) products.
- We may license an ISA (e.g. "ARMv8-A") or a specific microarchitectural implementation (e.g. "Cortex-A72")



…and our IP extends beyond the CPU

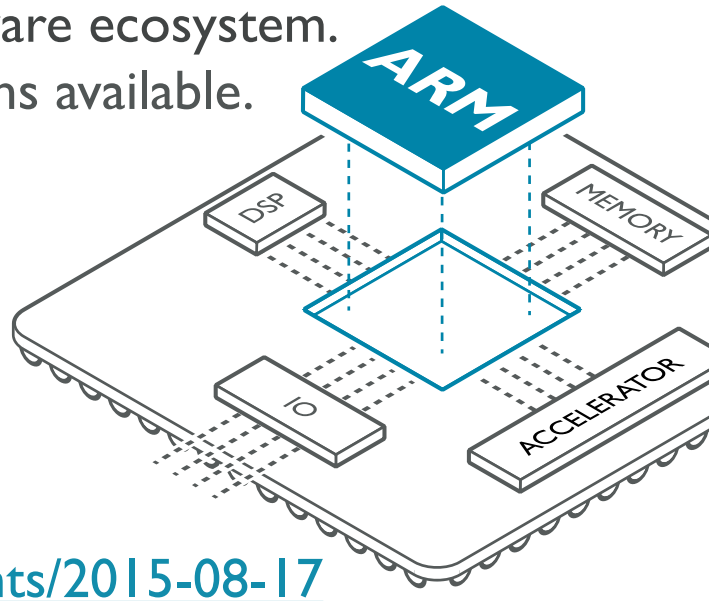
Why ARM in HPC?

Energy efficiency

- Energy has always been a first-class design constraint at ARM, the goal in our uArchitecture IP is to maintain that power efficiency advantage as we increase performance. The CPU core is only one element of the equation, we are also working to explore efficiency in the memory and on-chip interconnect space.

Choice

- Independent silicon providers within a shared software ecosystem.
- Wide range of price/performance/power/size options available.



Customisation

- ARM's partners can build SoCs very quickly.
- Getting interesting in the US:
  - SoC for HPC: http://www.socforhpc.org
  - DARPA CRAFT: http://www.darpa.mil/news-events/2015-08-17

HPC Leadership: International Exascale Programs

- **United States**
  - **Data Movement Dominates**
  - **FastForward II**
  - **PathForward (proposals)**

- **Japan**
  - **ARM based Fujitsu Post-K supercomputer will be deployed to RIKEN**

- **European Union**
  - **Montblanc 1, 2, & 3**
  - **ExaNode**
  - **Hartree Centre Deployment**
  - **H2020-FET-HPC (proposals)**

- **China**
  - **Multiple licensees pursuing HPC oriented systems**

Expanding ARMv8 vector processing

- ARMv7 Advanced SIMD (*aka* ARM NEON instructions) now 12 years old
  - Integer, fixed-point and non-IEEE single-precision float, on *well-conditioned* data
  - 16×128-bit vector registers
- AArch64 Advanced SIMD was an evolution
  - Gained full IEEE double-precision float and 64-bit integer vector ops
  - Vector register file grew from 16×128b to 32×128b
- New markets for ARMv8-A are demanding more radical changes
  - ✓ Gather load & Scatter store
  - ✓ Per-lane predication
  - ✓ Longer vectors
- But what is the preferred vector length?

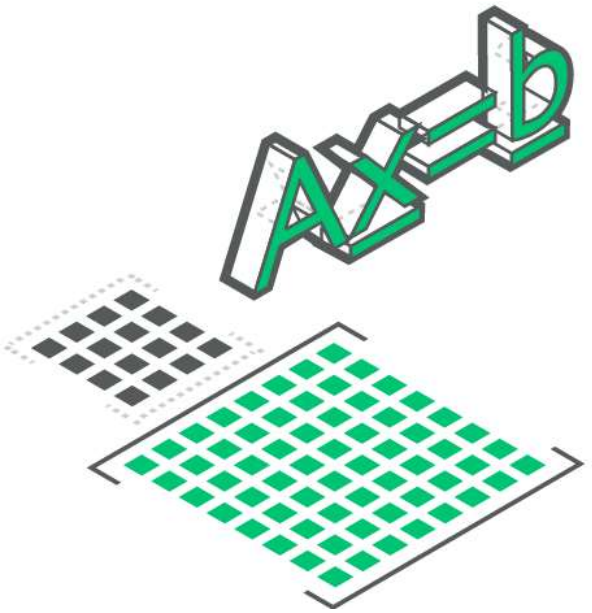
Introducing the Scalable Vector Extension (SVE)

- There is no preferred vector length
  - Vector Length (VL) is hardware choice, from 128 to 2048 bits, in increments of 128
  - *Vector Length Agnostic* (VLA) programming adjusts dynamically to the available VL
  - No need to recompile, or to rewrite hand-coded SVE assembler or C intrinsics

- SVE is not an extension of Advanced SIMD
  - A separate architectural extension with a new set of A64 instruction encodings
  - Focus is HPC scientific workloads, not media/image processing

- Amdahl says you need high vector utilisation to achieve significant speedups
  - Compilers often unable to vectorize due to intra-vector data & control dependencies
  - SVE also begins to address some of the traditional barriers to auto-vectorization

ARM Performance Libraries



Enable the wide variety of ARM cores available today without adding complexity to the software ecosystem.

- Commercially supported 64-bit ARMv8 vendor math libraries for scientific computing.
- Built and validated using technology from the Numerical Algorithms Group (NAG).
- ARM silicon partners provide us with tuned kernels.

Capabilities:

- BLAS
- LAPACK
- FFT

Tuned for:

- Cortex-A57,
- Applied Micro X-Gene®
- Cavium® ThunderX

ARM & OpenHPC

Participation:

- Silver member of OpenHPC
- ARM is on OpenHPC TSC in order to drive ARM architecture build support
- OpenHPC defines a clear target baseline of codes, many of which have already ported and are available on ARM. See **developer.arm.com/hpc** for details.

Status:

- 131 out of 166 packages building (79%)
- Closing on fixing remaining relevant packages and moving towards continous build integration on multiple ARM platforms

Functional Areas	Components
Base OS	RHEL/CentOS 7.1, SLES 12
Administrative Tools	Conman, Ganglia, Lmod, LosF, ORCM, Nagios, pdsh, prun
Provisioning	Warewulf
Resource Mgmt.	SLURM, Munge. Altair PBS Pro*
I/O Services	Lustre client (community version)
Numerical/Scientific Libraries	Boost, GSL, FFTW, Metis, PETSc, Trilinos, Hypre, SuperLU, Mumps
I/O Libraries	HDF5 (pHDF5), NetCDF (including C++ and Fortran interfaces), Adios
Compiler Families	GNU (gcc, g++, gfortran)
MPI Families	OpenMPI, MVAPICH2
Development Tools	Autotools (autoconf, automake, libtool), Valgrind,R, SciPy/NumPy
Performance Tools	PAPI, Intel IMB, mpiP, pdtoolkit TAU

International Standards

OpenDataPlane.org

JEDEC

HSA FOUNDATION

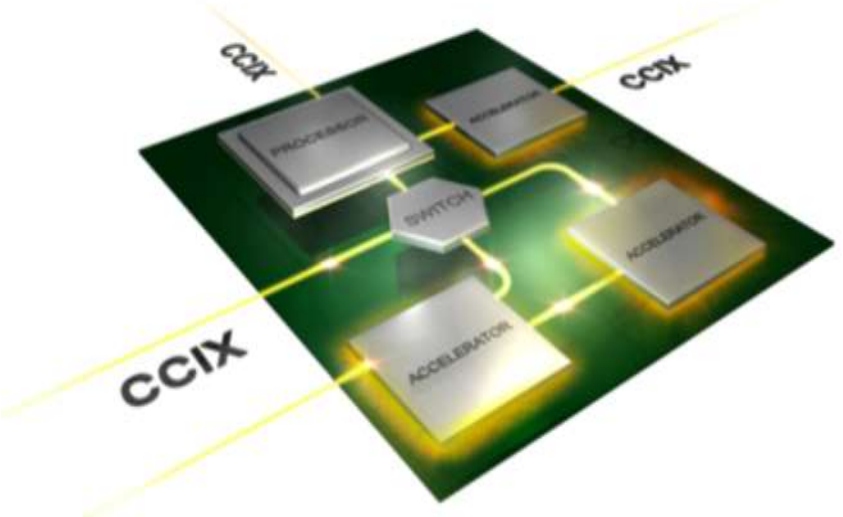
AMD ARM Imagination MEDIATEK QUALCOMM SAMSUNG

OPEN Compute Project

ARM AMBA Interconnect Standards

OpenMP

UCX Unified Communication X



ALTERA now part of Intel ARM IBM Micron

Hybrid Memory Cube CONSORTIUM

Open-Silicon SAMSUNG SEMTECH SK hynix XILINX

AMD ARM HUAWEI IBM

OpenSHMEM

Mellanox TECHNOLOGIES QUALCOMM XILINX ALL PROGRAMMABLE

Developer website : arm.com/hpc

ARM have launched an HPC-specific microsite

This is home to our HPC ecosystem offering:

- technical reference material
- how-to guides
- latest news and updates from partners
- downloads of HPC libraries
- third-party software recommendations
- web forum for community discussion and help

Participate and help drive the community