HC-1 Hybrid Core Computing

Applications

Convey Compilers

x86_64 instructions

coprocessor instructions

Cache-coherent shared virtual memory
Compiler code generation techniques

- Convey uses a different approach
  - Predefined machine state models (personalities)
  - Focus on a single thread to run much faster
  - Programmer productivity
    - “Dusty deck”
Embedded global memory

• Convey scales as the industry scales
  – Leverage multi-core and many-core x86 technologies
  – Global shared 64 bit virtual memory

• As the Convey architecture scales out ...
  – Look at PGAS languages
    • UPC
    • Co-Array Fortran
  – Multi level vectorization and parallelism

• Data placement directives are provided
• Data placement tool provided
Compiler Intermediate Format

• Standards are important to customers
  – ANSI C/C++
  – ANSI Fortran 95

• Known style for writing vectorizable code

• Directives are available

• Tuned libraries are available

• Instruction sets by industry or customer
  – Compiler utilizes specialized instructions when present
  – Predefined instruction sets provided by Convey
Hybrid systems or processor extensions
Run-time libraries

• A shared high level math library is provided
  – BLAS, LAPack, FFTs
  – Key routines are highly optimized

• Unmodified programs can dynamically link
  Convey math library
  – Optimized routines
  – Industry or customer specific instruction sets