WORKING BEYOND
MOORE’S LAW

INTEGRATION
- Multi-Chip Architectures
- 2 / 2.5 / 3D Packaging
- Scalable Fabrics

SYSTEM DESIGN
- Accelerators
- New Memory Architectures
- Advanced Interconnects

SOFTWARE
- Open Source
- Frameworks
- Coherency
**MULTIChip ARCHITECTURE REVOLUTION**

Monolithic die → Multi-die MCM → Chiplet
CHIPLETS

- More Silicon per Processor
- Each IP in its Optimal Technology
- Permits Rapid Architectural Innovation
- Optimized to Improve Latency and Power
- Enabled by Innovative Fabrics
MEMORY INNOVATION

Driving More DDR4 Memory Channels / Socket

Enabling At-Speed Memory Encryption for Unrivaled Security

On-Chip Stacked Memory (HBM2) Enables Highest Bandwidth Memory Subsystem (1 TB/S)

On-Die 3D Stacked Memory in Development

Die Stacking and 2.5D Integration
A COHERENT FUTURE

CPU, Accelerators, Fabrics, I/O

Sharing a Coherent Pool of Memory

COMING SOON...
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