Atos ARM solutions for HPC

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Tuesday, March 7th, HPC User Forum, TERATEC
Atos HPC and ARM
A long time engagement

Proof of concept: HPC computing based on mobile embedded technology

Extend the concept and explore new possibilities

- Prepare an industrial solution
- Test market acceptance

ARM Blades for Sequana
### Current processors technology snapshot

**Different suitespots for different workloads**

<table>
<thead>
<tr>
<th></th>
<th>Intel®</th>
<th>AMD®</th>
<th>ARM®</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Model considered</strong></td>
<td>Gold Skylake</td>
<td>Epyc Naples</td>
<td>Marvell ThX2</td>
</tr>
<tr>
<td><strong>Processing elements</strong></td>
<td>Up to 28 cores</td>
<td>Up to 32 cores</td>
<td></td>
</tr>
<tr>
<td><strong>Frequency</strong></td>
<td>2.0 – 2.7 GHz</td>
<td></td>
<td></td>
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<tr>
<td><strong>Max ISA supported</strong></td>
<td>AVX-512</td>
<td>AVX2</td>
<td>Neon</td>
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<tr>
<td><strong>DP FLOP/cycle</strong></td>
<td>2 FMA @ 512-bits</td>
<td>(2 ADD + 2 MUL) @ 128-bits</td>
<td>2 FMA @ 128-bits</td>
</tr>
<tr>
<td></td>
<td>32 FLOP/cycle</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Core DP FLOP/s</strong></td>
<td>64 GFLOP/s @ 2.0GHz</td>
<td>16 GFLOP/s @ 2.0GHz</td>
<td></td>
</tr>
<tr>
<td><strong>Socket DP FLOP/s</strong></td>
<td>1,792 GFLOP/s @ 2.0GHz</td>
<td>512 GFLOP/s @ 2.0GHz</td>
<td></td>
</tr>
<tr>
<td><strong>Memory Interface</strong></td>
<td>6 DDR4 channel @2667 MT/s</td>
<td>8 DDR4 channel @2667 MT/s</td>
<td></td>
</tr>
<tr>
<td><strong>Memory Bandwidth</strong></td>
<td>128 GByte/s/socket</td>
<td>170 GByte/s/socket</td>
<td></td>
</tr>
<tr>
<td><strong>Bytes:FLOP (1/Al)</strong></td>
<td>0.072</td>
<td></td>
<td>0.332</td>
</tr>
</tbody>
</table>
CN99xx: 1st member of **THUNDERX2** family

- Up to 32 custom ARMv8 cores, up to 2.5GHz
- Quad issue fully out of order, 4 threads per core
  - 32KB L1 I/D Cache; 256KB L2 per core
  - 32 MB distributed L3 cache (1MB per core)
  - 600 Gbps Gen 2 Coherent Processor Interconnect (CCPI2) (24 lanes @ 25Gbps)
  - 6 Tbps of on-die fabric for data (512 bits bidirectional running up to 3 GHz)
- Dual socket configuration support
- Up to 8 channels of DDR4, up to 2667MHz
- Up to 56 lanes of PCIe Gen3
- Integrated SATAv3, USB 3.0, GPIOs
- Server class virtualization
- Server class RAS
- Extensive Power Management
- Socketed LGA for most flexibility
Bull sequana compute blade: X1310
Marvell ThunderX2™ CN99xx – ARMv8 processor

- **1U form factor**
- **Direct liquid cooling**
- **3 compute nodes per blade with:**
  - 2 Marvell ThunderX2 processors with
    - Up to 32 custom ARMv8 cores per CPU, 4 threads per core, up to 2.5GHz
  - 16 DDR4 @266MT/s DIMM slots up to 1TB RAM
  - 1 Interconnect mezzanine board (EDR/HDR)
  - disks
    - 1 x 2.5” 7 mm SATA SSD
    - Or 1x 2.5” PCIe flash SSD
Atos Sequana Solutions Roadmap & ARM

- **Sequana X1000** (2018)
- **Sequana X1000 NG** (2019)
- **Intel Skylake**
- **NVIDIA Volta**
- **ThunderX2 B1** (2018)
- **ThunderX Next Gen** (2019)
- **SCS5 R1**
- **SCS5 R2**
- **SCS5 SI Phase 1**
- **SCS5 Single Island Phase 2**
- **ARM Compiler 6 & Tools**
- **Allinea Perf Report & Map**
- **MILO for ARM**
- **MILO enhanced for Sequana**

**Software Platform**

**X1000**

**X1000 NG**

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**Red Hat Certified Platform**

**ARM Compiler 6 & Tools**

**Allinea Perf Report & Map**

**MILO for ARM**

**MILO enhanced for Sequana**

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**GBL HPC & Quantum Solution | HPC User Forum – TERATEC – Bruyères-le-Châtel**
Integrate new usage models & new technologies
Matching emerging technologies and applications

1. Define a suitable & efficient ARM ecosystem for key customers workflows

2. Bring a clear strategy and directions to our future developments

3. Provide access to ARM resources and expertise
A full Solution to kickstart HPC projects on ARM

Be Efficient with Atos full spectrum solution

BullSequana X Family

First
Direct Liquid Cooled
ARM HPC solution

Enhanced support and porting lab expertise

X1000 & X1000 NG

ARM

MLO

ARM incubator labs

Atos
Thank you