AMD

EMERGING TECH PANEL: 3D MEMORY INTEGRATION

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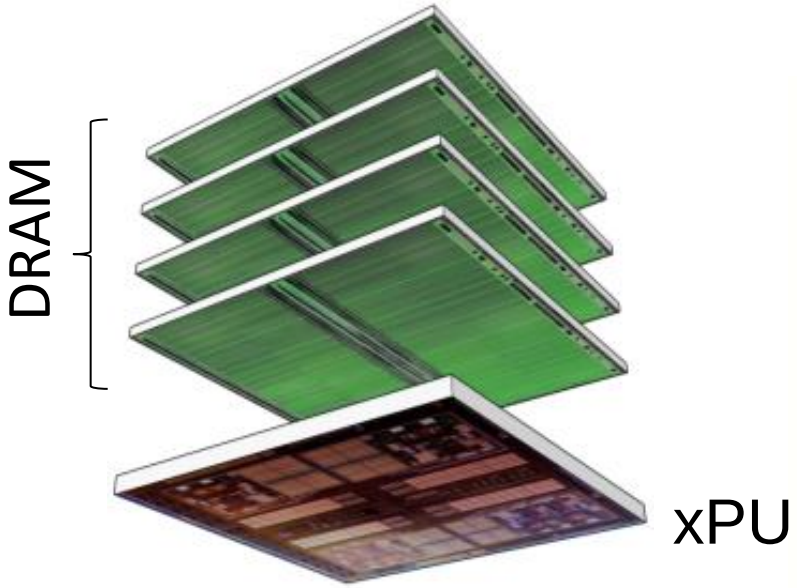
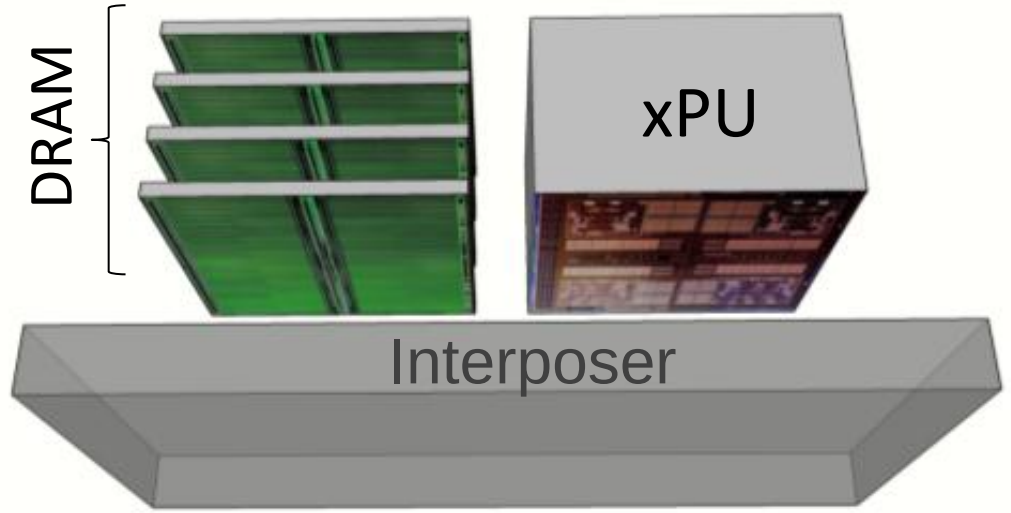
WHAT IS DIE-STACKING?



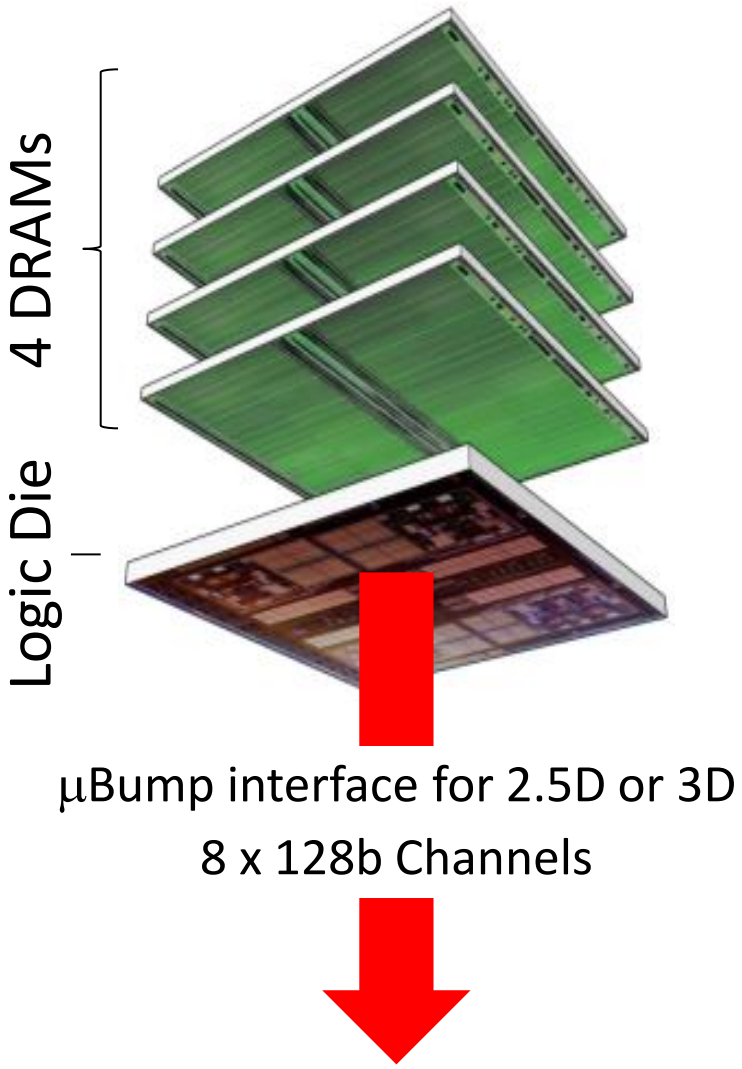


VERTICAL STACKING (3D) **INTERPOSER STACKING (2.5D)**

- Mix and match different technologies (e.g., CMOS, DRAM)
- Replace costly off-package interconnects with short, fast, low-energy in-package metal routes
- Increase integration density

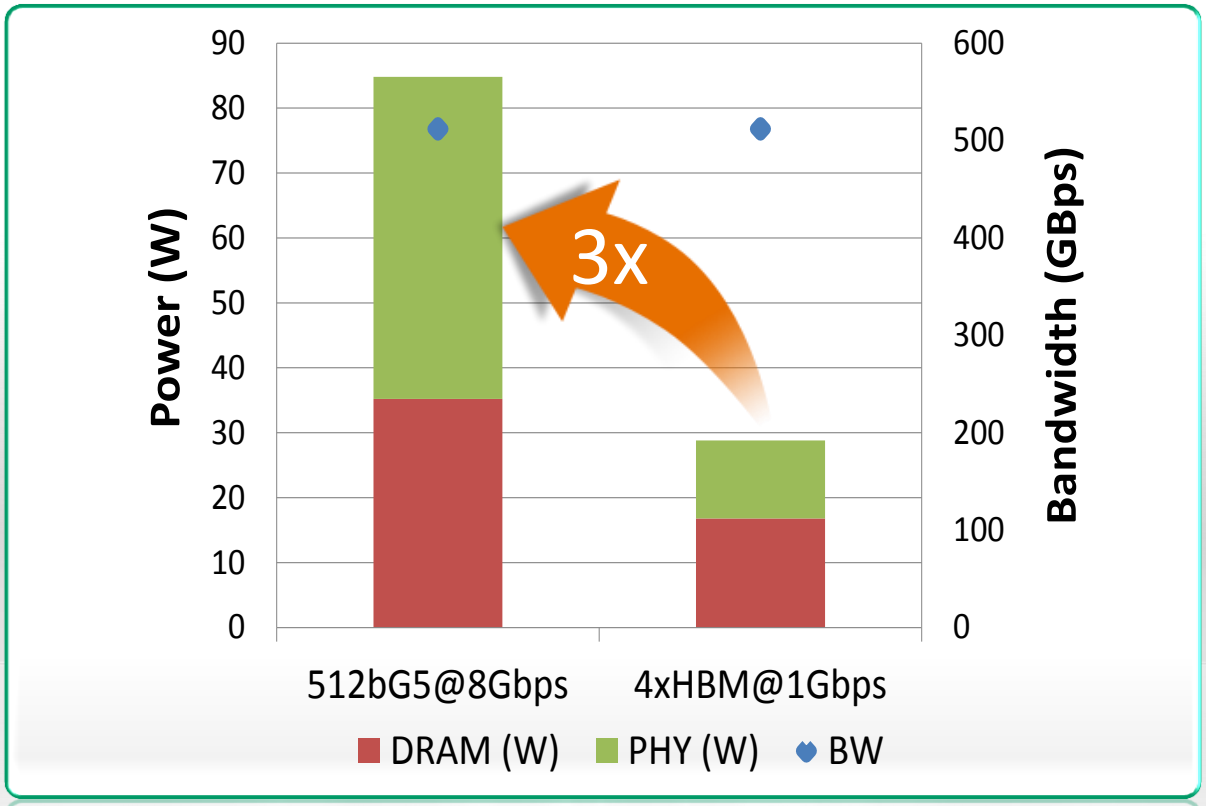
1ST GENERATION HBM IS SAMPLING!

HTTP://WWW.JEDEC.ORG/STANDARDS-DOCUMENTS/DOCS/JESD235



Voltage (I/O, VPP)	1.2V; 2.5V
Data Rate per pin	800 – 1.2 MT/s
DRAM Die Density	2Gb
DRAM Dies per Stack	4
Interface Width	1024
DQs/Channel	128
Channels/Die; Channels/Stack	2; 8
Address/Command Interface	DDR
Data Bus Clocking	Source synchronous; uni-directional/4byte
On Die DLL	No
Data Bus Termination – On die	No
Address/Cmd Termination – On die	No
DQ Training Mode	N/A
Page Size	2KB
Banks/Channel	8
DRAM Prefetch; Burst Length	256 bits; 2

IMPROVING BW/WATT WITH DIE-STACKED MEMORY



Source: AMD

- Die stacking improves the proximity of the DRAM to Compute
- Dense and fine pitch interconnect enables simple low power interfaces as well as fine grain power control of the DRAM

WHAT THIS MEANS FOR HPC

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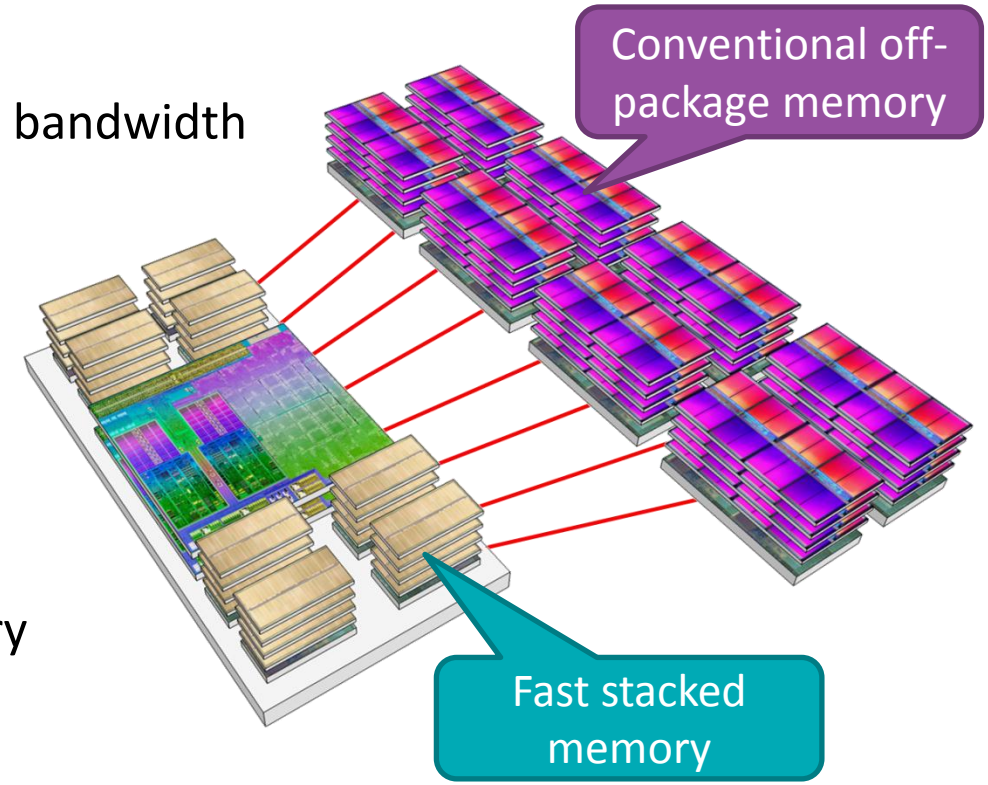
- In-package memory to deliver high bandwidth at low power cost
- But… in-package memory does not provide enough capacity
  - Still need conventional memory for capacity
- Results in a heterogeneous memory organization/hierarchy



- How does one make small-fast + large-slow memory act like a single, uniform large+fast memory?
  - Hardware? Software? Combination?

PANEL QUESTIONS

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- Q1: What is most needed to bring to market?
  - Hardware: technology is there, now need more volume to drive costs/risks down
  - Software: may be more evolutionary, multiple usage models
- Q2: What markets will use it first? Will it be mainstream?
  - Where bandwidth needs are the highest (GPU)
- Q3: What supporting technologies are required?
  - For wide adoption, software support needs to be there
  - System software development dependent on hardware availability
  - Applications optimization dependent on system software, runtimes, libraries, etc.
- Q4: What partners would help bring to market sooner?
  - SoC vendors using more stacked memory → volume
    - Enabled/enhanced by common standards (e.g., JEDEC HBM)
    - More platforms → more software development

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