EMERGING TECH PANEL:
3D MEMORY INTEGRATION

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WHAT IS DIE-STACKING?

- Mix and match different technologies (e.g., CMOS, DRAM)
- Replace costly off-package interconnects with short, fast, low-energy in-package metal routes
- Increase integration density

VERTICAL STACKING (3D)

INTERPOSER STACKING (2.5D)
**1st Generation HBM is Sampling!**

[HTTP:WWW.JEDEC.ORG/STANDARDS-DOCUMENTS/DOCS/JESD235](HTTP:WWW.JEDEC.ORG/STANDARDS-DOCUMENTS/DOCS/JESD235)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage (I/O, VPP)</td>
<td>1.2V; 2.5V</td>
</tr>
<tr>
<td>Data Rate per pin</td>
<td>800 – 1.2 MT/s</td>
</tr>
<tr>
<td>DRAM Die Density</td>
<td>2Gb</td>
</tr>
<tr>
<td>DRAM Dies per Stack</td>
<td>4</td>
</tr>
<tr>
<td>Interface Width</td>
<td>1024</td>
</tr>
<tr>
<td>DQs/Channel</td>
<td>128</td>
</tr>
<tr>
<td>Channels/Die; Channels/Stack</td>
<td>2; 8</td>
</tr>
<tr>
<td>Address/Command Interface</td>
<td>DDR</td>
</tr>
<tr>
<td>Data Bus Clocking</td>
<td>Source synchronous; uni-directional/4byte</td>
</tr>
<tr>
<td>On Die DLL</td>
<td>No</td>
</tr>
<tr>
<td>Data Bus Termination – On die</td>
<td>No</td>
</tr>
<tr>
<td>Address/Cmd Termination – On die</td>
<td>No</td>
</tr>
<tr>
<td>DQ Training Mode</td>
<td>N/A</td>
</tr>
<tr>
<td>Page Size</td>
<td>2KB</td>
</tr>
<tr>
<td>Banks/Channel</td>
<td>8</td>
</tr>
<tr>
<td>DRAM Prefetch; Burst Length</td>
<td>256 bits; 2</td>
</tr>
</tbody>
</table>

**Diagram:**

- 4 DRAMs
- Logic Die
- μBump interface for 2.5D or 3D
- 8 x 128b Channels
Die stacking improves the proximity of the DRAM to Compute

Dense and fine pitch interconnect enables simple low power interfaces as well as fine grain power control of the DRAM.
WHAT THIS MEANS FOR HPC

- In-package memory to deliver high bandwidth at low power cost
- But... in-package memory does not provide enough capacity
  - Still need conventional memory for capacity

- Results in a heterogeneous memory organization/hierarchy

- How does one make small-fast + large-slow memory act like a single, uniform large+fast memory?
  - Hardware? Software? Combination?
PANEL QUESTIONS

Q1: What is most needed to bring to market?
- Hardware: technology is there, now need more volume to drive costs/risks down
- Software: may be more evolutionary, multiple usage models

Q2: What markets will use it first? Will it be mainstream?
- Where bandwidth needs are the highest (GPU)

Q3: What supporting technologies are required?
- For wide adoption, software support needs to be there
- System software development dependent on hardware availability
- Applications optimization dependent on system software, runtimes, libraries, etc.

Q4: What partners would help bring to market sooner?
- SoC vendors using more stacked memory → volume
  - Enabled/enhanced by common standards (e.g., JEDEC HBM)
  - More platforms → more software development
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