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Advancing Science in Alternative Energy and Bioengineering with Many-Core Processors

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†Disclaimer: This talk includes results from my tenure at ORNL that do not necessarily reflect the views, research directions, etc. of Intel® Corporation.*

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Outline

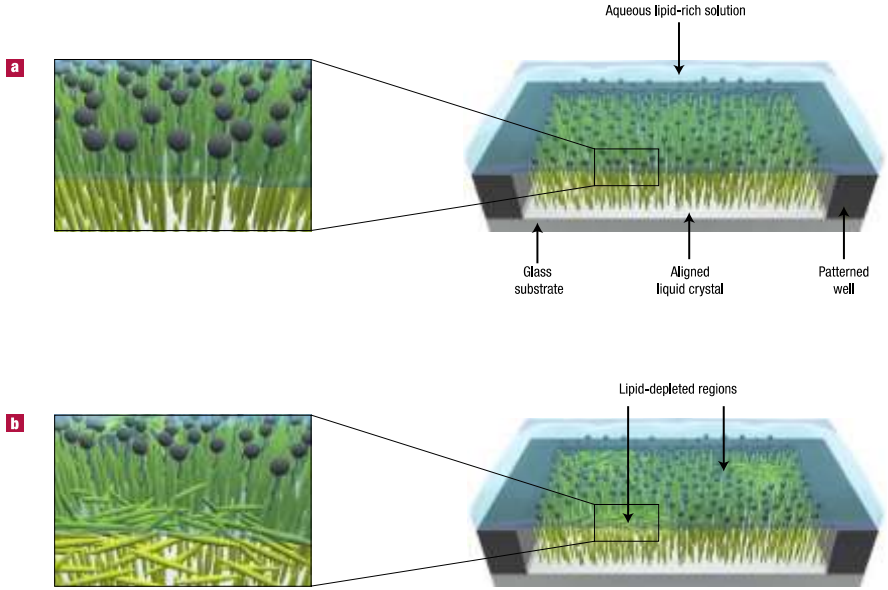
Motivation:	A subset of science problems I have been involved with that have been difficult to investigate with previous hardware/software solutions
What we have done:	Recent hardware and software advances that have enabled new investigations
What we are doing:	Issues and the solutions required to continue to advance HPC capabilities

3 Example Science Drivers

Liquid Crystal Biosensors

Label Free Diagnostics

- Alignment changes induced by interactions with biomolecules can be detected with optical microscopy
- *"Critical to this area is a sound understanding of the theory and modelling of liquid-crystal materials at interfaces. Computer simulations of the molecular and mesoscopic interactions between thermotropic liquid-crystal materials … are a necessity. It is important to understand the interactions at these complicated interfaces"* - Woltman, et al., *Nature Materials*,* 6, 929 (2007)
- Prior to 2013, no molecular simulations at experimentally relevant scales
  - Computational limitation
  - Extrapolations from small-scale studies difficult/dangerous due to the presence of undulative modes



Woltman, et al., *Nature Materials*,* 6, 929 (2007)

Icephobic Surfaces for Wind Power

Many of the regions of the world that can benefit from wind power are in cold climates

Ice can reduce the efficiency of turbines or force shutdown

Extremely difficult to probe ice formation experimentally

Probing with simulation requires large simulations at time scales sufficient to capture rare nucleation events leading to ice formation

Organic Solar Cells

Organic photovoltaic (OPV) solar cells are promising renewable energy sources

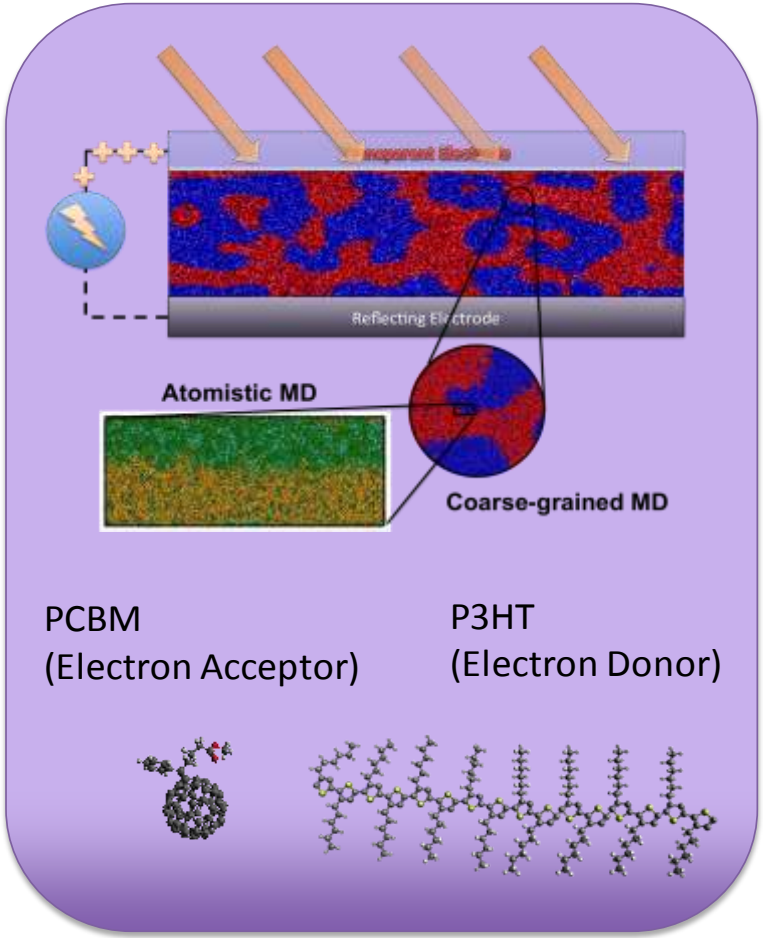
- Low cost, high-flexibility, light weight

Morphology of the OPV active layer has a significant impact on device efficiency

- Donor regions should be large enough to absorb light efficiently, but small enough to allow charge excitations to diffuse to acceptor before recombining
- High interface-to-volume ratio for efficient exciton dissociation
- Proper donor molecular alignment to optimize the carrier mobility of the donor phase

Multi-scale problem

- Very large simulations to reach experimental scales



Hardware and Software Advances

Many-core and GPUs

Issues with power consumption, heat dissipation, and memory access latencies have forced a change in direction towards many-core processors for current and next-generation supercomputers that advance the limits of peak floating point performance

GPU-based architectures were the first affordable many-core processors generally available

ORNL* Titan came online in late 2012 as a hybrid supercomputer capable of over 17PF HPL performance.

- Cray* XK7 architecture with a Gemini* network interconnect and nodes containing a single AMD* Opteron* 6274 processor and Nvidia* Tesla K20X

Center for Accelerated Application Readiness (CAAR at ORNL*)

In order to exploit the potential performance gains on Titan, changes to the software are required

CAAR was formed to address this issue for several codes before the upgrade to Titan

- LAMMPS* (Large-scale Atomic/Molecular Massively Parallel Simulator) was the molecular dynamics code chosen for CAAR
  - We implemented the 'GPU package' for LAMMPS* with new algorithms suited for running on hybrid GPGPU architectures

Brown, W.M., Wang, P. Plimpton, S.J., Tharrington, A.N. **Implementing Molecular Dynamics on Hybrid High Performance Computers - Short Range Forces**. *Computer Physics Communications**. 2011. 182: p. 898-911.
Brown, W.M., Kohlmeyer, A. Plimpton, S.J., Tharrington, A.N. **Implementing Molecular Dynamics on Hybrid High Performance Computers - Particle-Particle Particle-Mesh**. *Computer Physics Communications**. 2012. 183: p. 449-459.

Spinoidal Dewetting in Liquid Crystal Layers

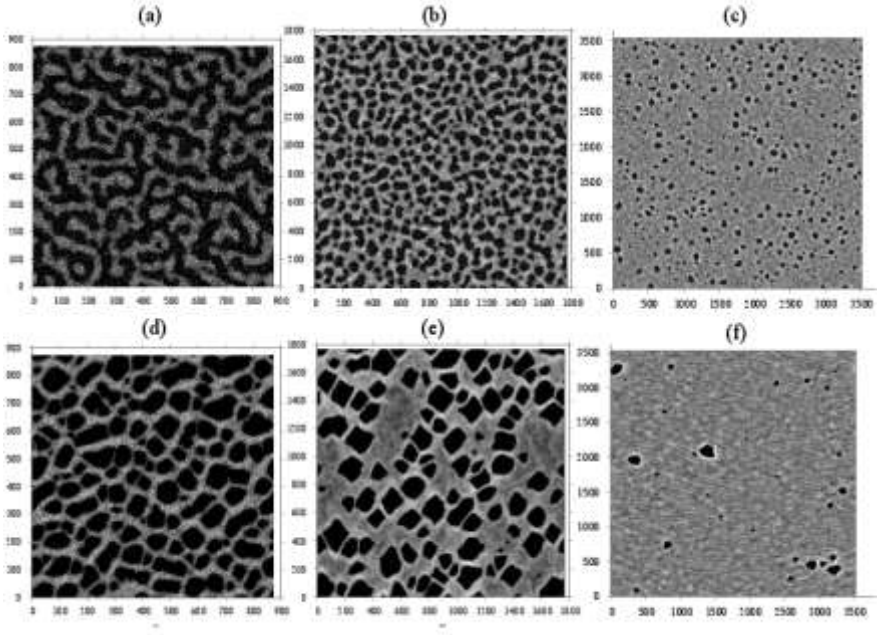
Science Team: Trung Dac Nguyen, Jan-Michael Carrillo, Mike Matheson, W. Michael Brown, (ORNL)*

***Problem**: How/why do defects form in liquid crystal layers?*

- Not possible to study on previous Jaguar supercomputer with software available unless the machine was dedicated to the problem

Innovation: Coarse-grain simulation model with high arithmetic intensity/vector potential, GPU algorithms

***Result**: > 7X performance gain (1S CPU+GPU vs 2S CPU); First simulations at scale with molecular detail*



Nguyen, T. D., Carrillo, J.-M. Y., Matheson, M. A., Brown, W.M., **Rupture Mechanism of liquid crystal thin films realized by large-scale molecular simulations**. *Nanoscale**. 2014. 6: 3083-96.

Icephobic Surfaces

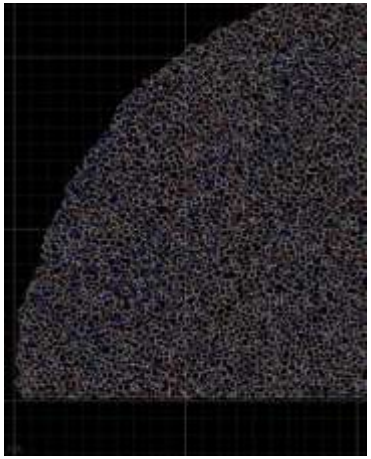
Science Team: Yamada Masako, et. al (GE Global Research)*

Problem: Probe mechanism for water droplet freezing on a surface with molecular detail

Innovation: New 3-body potential for water simulation (E. B. Moore, V. Molinero, *Nature** 479 (2011) 506–508)

- Coarse-grain model, eliminate all-to-all communications for electrostatics, larger timestep
  - > 100X Simulation rate speedup from model
- Additional concurrency for 3-body: O(N^3) independent force computations vs O(N^2)
  [for N *atoms within cutoff radius]*
  - Additional 2-3X Simulation speedup on XK7 node (1S CPU+GPU) vs 2S Opteron*

Result: Simulation of water freezing process now typical with hundreds of nodes.



Brown, W.M., Masako, Y. **Implementing Molecular Dynamics on Hybrid High Performance Computers – Three-Body Potentials.** *Computer Physics Communications**. 2013. 184: p. 2785-2793.

Issues with Hybrid GPU Machines

Issues with the Programming Model

Using CUDA* with C/C++ semantics introduces **multiple languages**, code paths, compiler requirements, etc. into a code base.

- Support for Fortran or x86 targets requires proprietary compilers

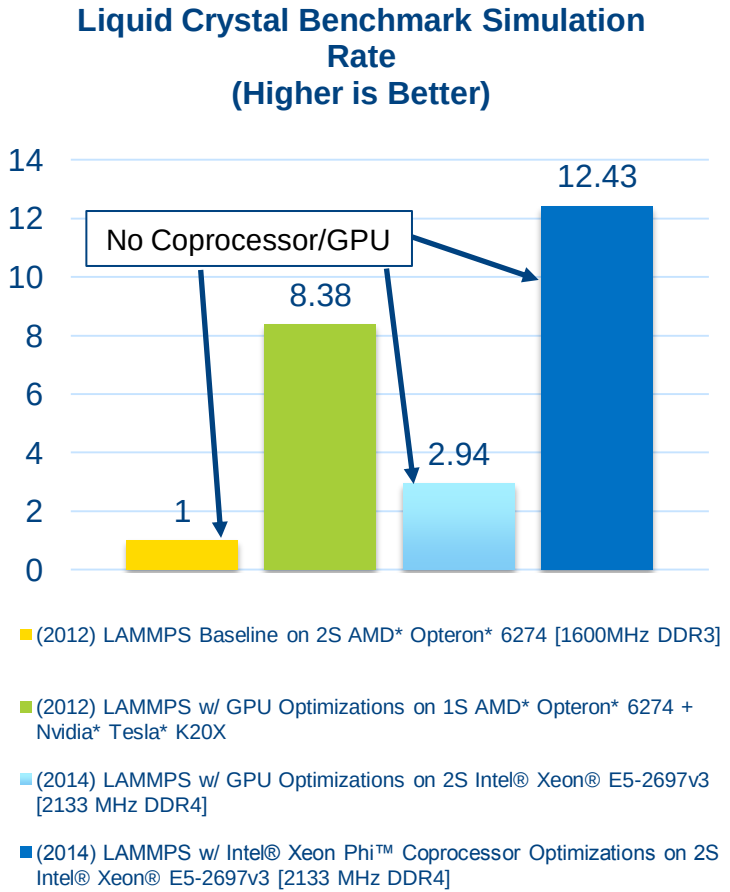
OpenACC* can potentially address this, but in my opinion, will still require **separate code paths** and **different algorithms** for x86 in general

- GPUs have 10,000s of threads in flight, different performance for atomic operations, different penalties for thread synchronization, context switching, etc.
- For example, the algorithms used for molecular dynamics on the GPU would not perform well on x86 processors.
  - For the 3-body water/ice simulation presented here, we *triple* the number of force computations on the GPU with redundant computations!

Optimizing separate code paths

Optimizations for GPU do not necessarily improve performance on CPUs

- Many production codes supporting GPU acceleration still use the CPU for many routines and must still support CPU-only
- Intel® Xeon® processors are still improving the performance/socket
- 85% of all systems on TOP500* use Intel® processors (97% of new systems)
- Future Intel® many-core processors will be bootable (no coprocessor necessary)
- Difficult to manage/debug/port software with separate optimization code paths



Source:
AMD* & AMD/NVIDIA* results: http://www.nvidia.com/docs/IO/122634/computational-chemistry-benchmarks.pdf
Intel Results: Intel Measured August 2014

Intel® Package for LAMMPS

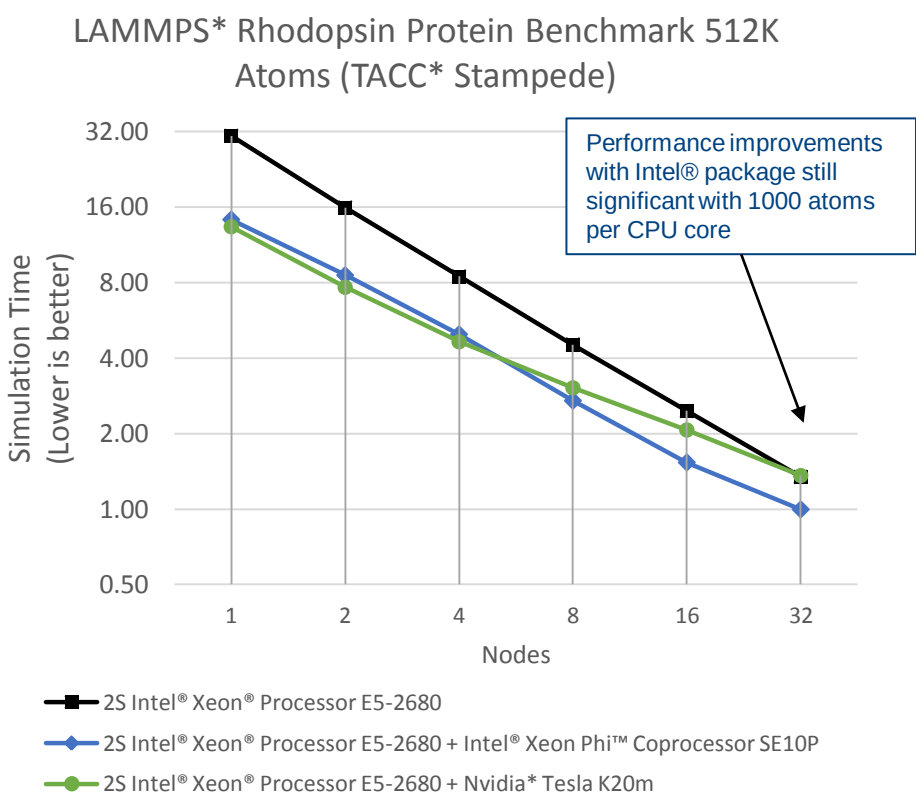
Motivation

Provide a workspace for demonstrating code modernization strategies with vectorization for different precision modes, OpenMP*, and MPI*-3

Support computation offload to Intel® coprocessors with performance that is comparable or better than GPU performance

Demonstrate portable performance with a single code path using standard MD algorithms with C++/OpenMP*

Provide routines that allow the community to easily add new functionality by example



Stampede Configuration: HT Off, 32GB DDR3-1600MHz, PCIe2 (GPU), PCIe2 (Intel® Coprocessor), FDR 56 Gb/s, MPSS 3.3, MVAPICH 2.0b

Source: Intel Measured August 2014

Current Optimizations in Intel Package

Data alignment

Support for mixed and single precision modes in addition to double

SIMD directives to allow compiler vectorization for routines with data dependencies

Modifications to conditional branches to better support compiler vectorization for both coprocessors and Intel® Advanced Vector Extensions (Intel® AVX)

Neighbor-list padding to prevent execution of vector remainder code

Offload directives to manage data allocation, transfer, and concurrent computation on the coprocessor

Advantages of Intel® Package vs GPU Package (1)

- Same code for routines run on the CPU and coprocessor (with or without offload)
  - Optimizations for Intel® Xeon Phi™ coprocessors resulted in faster performance on Intel® Xeon® processors (up to 3.5X)
  - GPU package uses ***different algorithms*** and different code/language
- Support for both ‘newton’ settings allows for more flexibility for new force-fields
- Improved flexibility for heterogeneous calculations
  - Intel® coprocessor offload not limited to 16 MPI* tasks on CPU (CUDA*-MPS limitation)
  - Intel® package supports OpenMP* with multiple threads on the CPU (GPU package does not use OpenMP)
  - MPI* tasks sharing coprocessor are able to get exclusive core affinity

Advantages of Intel® Package vs GPU Package (2)

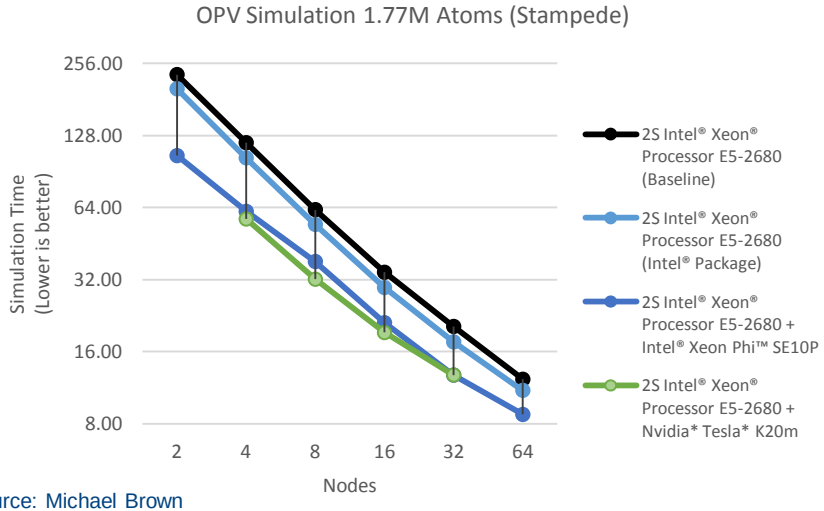
- More options for overlap of MPI* communications and computation
- Build process is simpler and does not require building a separate library for coprocessor routines
  - One compiler/Makefile for everything
- Precision mode (single, mixed, or double) can be switched at run-time without rebuilding
- Package written in standard C++ with OpenMP*
  - Offload directives used for the coprocessor

Organic Solar Cells

Science Team: Jan-Michael Y Carrillo, Rajeev Kumar, Monojoy Goswami, S. Michael Kilbey II, Bobby G Sumpter (ORNL/UT*)*

Problem: Predictive simulation of active layer morphology and molecular alignment based on blend composition

Innovation: Code Modernization/HW



Source: Michael Brown

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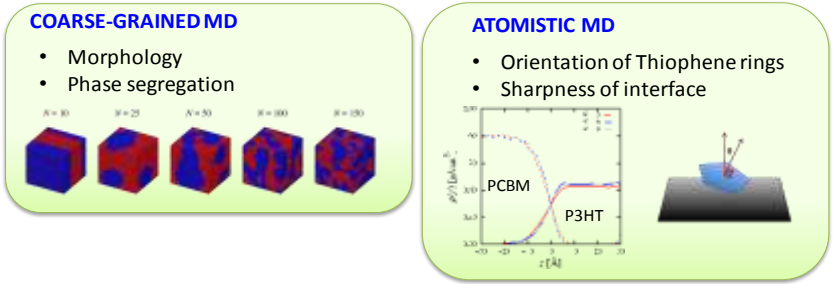
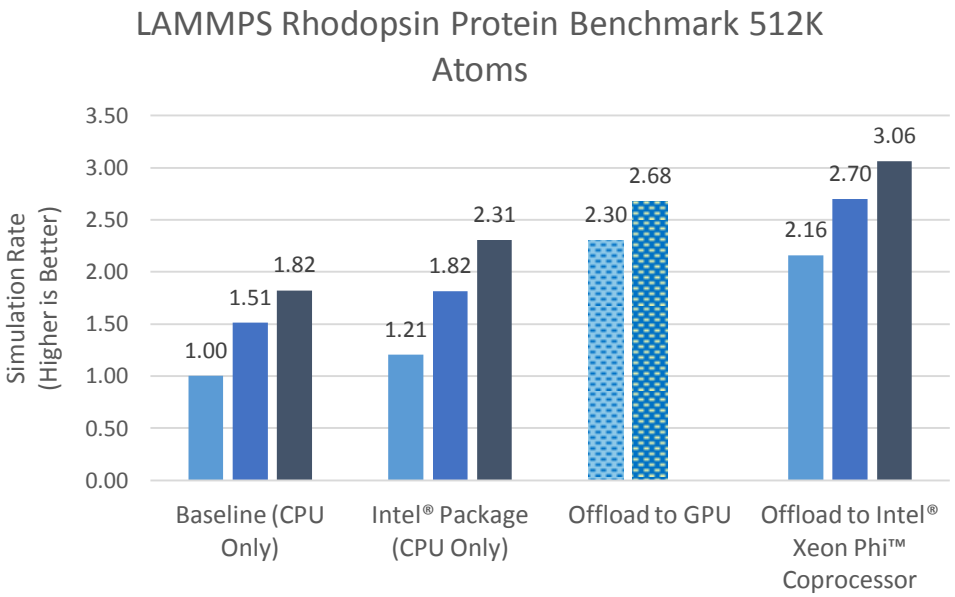
Result: With code modernization and advanced HPC resources, we have been the first to perform simulations at scales that match experiment.

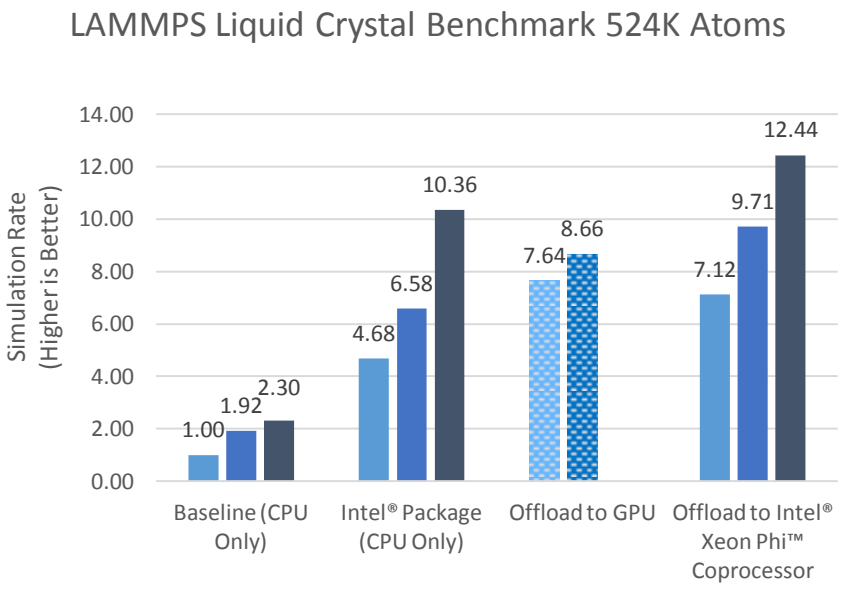
- *Left:* Up to 1.9X with use of a coprocessor
  - *Simulations include all of the statistics and I/O (about 10% of run time) from the production runs*
- Significant potential for advanced multiscale simulation models with coprocessors…



Carrillo, J.-M. Y., Kumar, R., Goswami, G., Sumpter, B., Brown, W.M., **New Insights into Dynamics and Morphology of P3HT:PCBM Active Layers in Bulk Heterojunctions**. *Physical Chemistry Chemical Physics*. 2013. 15: p. 17873-17882.

LAMMPS performance with current processors





2S Intel® Xeon® Processor E5-2680 / Nvidia* Tesla* K20m / Intel® Xeon Phi™ Coprocessor SE10P†

2S Intel® Xeon® Processor E5-2697v2 / Nvidia* Tesla* K40c / Intel® Xeon Phi™ Coprocessor 7120A ‡

2S Intel® Xeon® Processor E5-2697v3 / HW Not Available / Intel® Xeon Phi™ Coprocessor 7120A‡

Issues/Improvements

Available/Ongoing/Future Improvements

Compiler vectorization

- Significant advances in compiler vectorization using the Intel® Composer XE 2015.
- *New:* Vector variant functions that allow explicit vector coding for small subroutines
- Advanced compiler optimization reports with Intel® Composer XE 2015 and runtime analysis with Intel® VTune™ Amplifier XE

MPI Performance in symmetric modes

- Significant performance improvements with Intel® MPI* 5.
- Future many-core chips will have bootable options and also options for integrated fabric

Unveiling Details of Knights Landing

(Next Generation Intel® Xeon Phi™ Products)

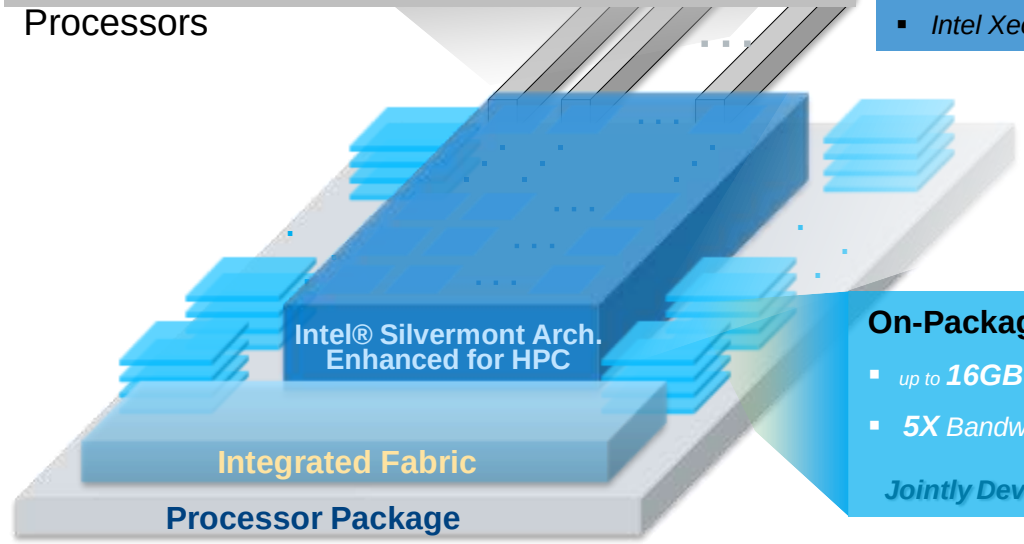
2nd half '15
1st commercial systems

3+ TFLOPS[1]
In One Package
Parallel Performance & Density

Platform Memory: DDR4 Bandwidth and Capacity Comparable to Intel® Xeon® Processors

Compute: Energy-efficient IA cores[2]

- *Microarchitecture enhanced for HPC[3]*
- ***3X** Single Thread Performance vs Knights Corner[4]*
- *Intel Xeon Processor Binary Compatible[5]*



On-Package Memory:

- *up to **16GB** at launch*
- ***5X** Bandwidth vs DDR4[7]*
- ***1/3X** the Space[6]*
- ***5X** Power Efficiency[6]*

Jointly Developed with Micron Technology

Designed using Intel's cutting-edge
14nm Transistor Technology

Not bound by "offloading" bottlenecks
Standalone CPU or PCIe Coprocessor

Common instruction set architecture
Intel® Advanced Vector Extensions 512

All products, computer systems, dates and figures specified are preliminary based on current expectations, and are subject to change without notice. [1]Over 3 Teraflops of peak theoretical double-precision performance is preliminary and based on current expectations of cores, clock frequency and floating point operations per cycle. FLOPS = cores x clock frequency x floating-point operations per second per cycle. . [2]Modified version of Intel® Silvermont microarchitecture currently found in Intel® Atom™ processors. [3]Modifications include AVX512 and 4 threads/core support. [4]Projected peak theoretical single-thread performance relative to 1st Generation Intel® Xeon Phi™ Coprocessor 7120P (formerly codenamed Knights Corner). [5] Binary Compatible with Intel Xeon processors using Haswell Instruction Set (except TSX) . [6]Projected results based on internal Intel analysis of Knights Landing memory vs Knights Corner (GDDR5). [7]Projected result based on internal Intel analysis of STREAM benchmark using a Knights Landing processor with 16GB of ultra high-bandwidth versus DDR4 memory only with all channels populated.

Conceptual—Not Actual Package Layout

Summary

Summary

We have demonstrated that important research for a variety of science problems continues to benefit from hardware and software advances in HPC.

We believe that the Intel® path forward for HPC architecture and software solutions is superior

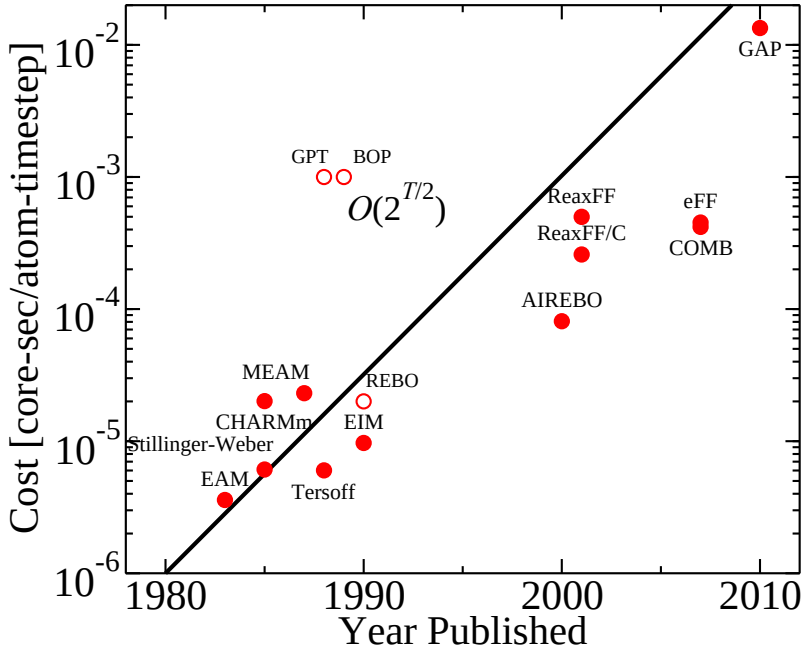
- We are dedicated to providing solutions that allow for portable performance across a range of different processors for both conventional HPC centers and those on a path to exa-scale.

We have demonstrated, in a large production code, that optimizations for Intel® Xeon Phi™ coprocessors also improve performance on Intel® Xeon® processors and that the same routine can be used for efficient computations on both

Summary (2)

The innovations here also included reconsideration of the simulation model

- Important to realize that there is often a choice in the model used, and that in the past, minimizing computation was important to performance
- It may be the case that you can exploit additional arithmetic intensity and concurrency to increase the accuracy, time-step, etc. in order to advance research capabilities
  - This has already been the case for simulation in materials problems



Computational Aspects of Many-body Potentials, S. J. Plimpton and A. P. Thompson, *MRS Bulletin**, 37, 513-521 (2012).

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DOE Early Science and ALCC Programs

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NSF TACC* Stampede Project: ACI-1134872

The researchers acknowledge the Texas Advanced Computing Center (TACC) at The University of Texas at Austin* for providing HPC resources that have contributed to the research results reported within this paper. URL: http://www.tacc.utexas.edu*

NSF UT* Beacon Project

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