# **In-Network Computing**

Paving the Road to Extreme Scale Computing October 2019







## **The Need for Intelligent and Faster Interconnect**

Faster Data Speeds and In-Network Computing **Enable Higher Performance and Scale** 



Must Wait for the Data **Creates Performance Bottlenecks** 



Analyze Data as it Moves CPUs, CPU and IPUs (I/O Processing Units) **Higher Performance and Scale** 





### **Data Centric Architecture to Overcome Latency Bottlenecks**

Intelligent Interconnect Paves the Road to Exascale Performance



**Communications Latencies** of 30-40us



**Communications Latencies** of 3-4us







# **IPU Technologies: Scalable Hierarchical Aggregation and Reduction Protocol (SHARP)**



### Scalable Hierarchical Aggregation and Reduction Protocol (SHARP)

Reliable Scalable General Purpose Primitive

- In-network Tree based aggregation mechanism
- Large number of groups
- Multiple simultaneous outstanding operations
- Applicable to Multiple Use-cases
  - HPC Applications using MPI / SHMEM
  - Distributed Machine Learning applications

Scalable High Performance Collective Offload

- Barrier, Reduce, All-Reduce, Broadcast and more
- Sum, Min, Max, Min-loc, max-loc, OR, XOR, AND
- Integer and Floating-Point, 16/32/64 bits





### **SHARP AllReduce Performance Advantages (128 Nodes)**

**Allreduce Latency** 50.00 10.00 9.00 45.00 8.00 40.00 7.00 35.00 Latency (usec) ក្ត 30.00 6.00 5.00 25.00 4.00 20.00 3.00 ŋ 15.00 10.00 2.00 1.00 5.00 0.00 0.00 16 16 32 128 2 4 8 2 4 8 64 Cluster Size (Nodes) Cluster Size (Nodes) SHARP - 8B SHARP - 128B — Software - 8B Software - 128B SHARP - 1024B SHARP - 2048B









### **SHARP AllReduce Performance Advantages** 1500 Nodes, 60K MPI Ranks, Dragonfly+ Topology (University of Toronto)



HPC-X SHARP Software MPI

HPC-X SHARP Software MPI



### **NCCL-SHARP Delivers Higeher Performance**

Mellanox SHARP Plug-in for NCCL 2.4 (Bandwidth)







# **IPU Technologies: MPI Tag Matching Hardware Engine**





### Tag Matching Hardware Engine Performance Advantage



**MPI Latency (Eager)** 

**MVAPICH2** 





Courtesy of Dhabaleswar K. (DK) Panda **Ohio State University** 



### -MVAPICH2+HW-TM

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# **Network Topologies** Leveraging Multi-Host Technology



### **Supporting Variety of Topologies**







## Mellanox Multi-Host<sup>™</sup> Technology

- Mellanox Multi Host<sup>®</sup> technology enables connecting multiple hosts into a single interconnect adapter
- By separating the ConnectX PCIe interface into multiple and independent PCIe interfaces
- Each interface is connected to a separate host with no performance degradation
- Increase datacenters performance while reducing CAPEX and OPEX





## Facebook OCP Multi-Host Platform (Yosemite)





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### **ConnectX External Multi Host**





P28 DOGBE	commette	
	PCIe Gen3/4 x4 (electrical)	-
	3x Daughter cards	
	Dolimor Freedad	
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### Power, space and management savings



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### **Higher Server Performance with Socket Direct**

- Overcomes CPU to CPU connectivity bottleneck
- Ensure optimal performance on both CPU sockets
- Enable GPUDirect Technology from both CPU PCI root Complex









## **HDR InfiniBand and**





### **Highest-Performance 200Gb/s InfiniBand Solutions**

Adapters	ConnectX·6	200Gb/s Adapter, 0.6us latency 215 million messages per second (10 / 25 / 40 / 50 / 56 / 100 / 200Gb/s)	
Switch	Mellanox: Quantum-∯	40 HDR (200Gb/s) InfiniBand Ports 80 HDR100 InfiniBand Ports Throughput of 16Tb/s, <90ns Latency	S
SOC	BlueField <sup>*</sup> -2	System on Chip and SmartNIC Programmable adapter Smart Offloads	
Interconnect	·Link	Transceivers Active Optical and Copper Cables (10 / 25 / 40 / 50 / 56 / 100 / 200Gb/s)	(
Software	· HPC-X·	MPI, SHMEM/PGAS, UPC For Commercial and Open Source Applications Leverages Hardware Accelerations	





## **BlueField-2 Block Diagram**

Tile architecture running 8 x Arm <sup>®</sup> A72 CPUs

- SkyMesh<sup>™</sup> coherent low-latency interconnect
- 6MB L3 Last Level Cache
- Arm frequency : 2GHz 2.5GHz
- Up to 200Gb/s port bandwidth, InfiniBand or Ethernet
  - ConnectX-6 based
- Acceleration engines
  - ASAP2 switching and packet processing
  - NVMe SNAP<sup>™</sup> storage emulation
  - IPsec/TLS data-in-motion and AES-XTS
  - Data-at-rest crypto accelerations
- Fully integrated PCIe switch
  - PCIe Gen3/4





## **The New Architecture Vision: Bring RDMA All the Way to the Edge**





### The Edge





