LEADING THE EVOLUTION OF COMPUTE

MARK KACHMAREK
HPC STRATEGIC PLANNING MANAGER
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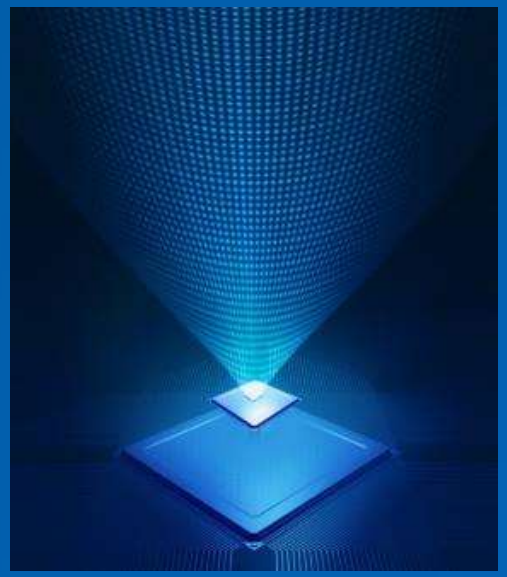
INTEL'S RESEARCH EFFORTS

COMPONENTS RESEARCH

ENABLING MOORE'S LAW



DEVELOPING NOVEL INTEGRATION

INTEL LABS

ENABLING FUTURE PRODUCT CAPABILITIES

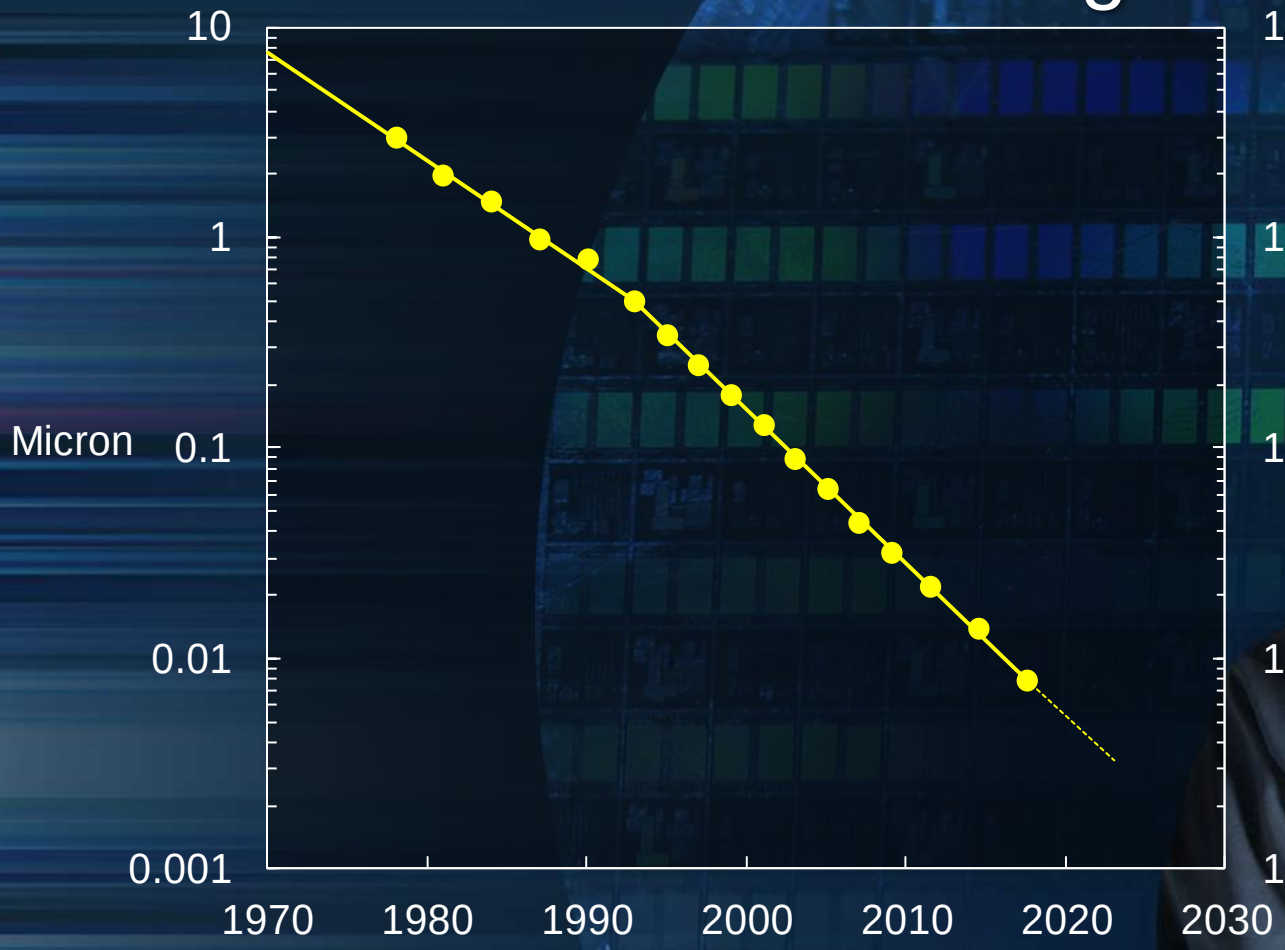
ANTICIPATING FUTURE INTEL

UNIVERSITY RESEARCH

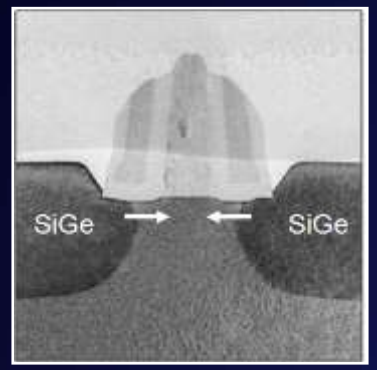
Expanding the Frontier, Future Intel Collaborators

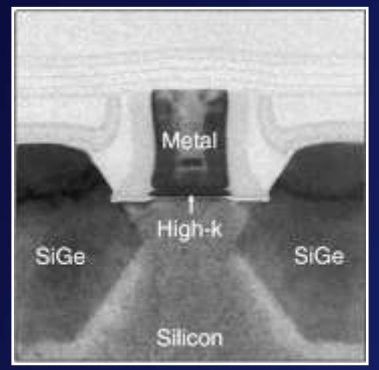

“The number of transistors and resistors on a chip doubles every 24 months”
-Gordon Moore

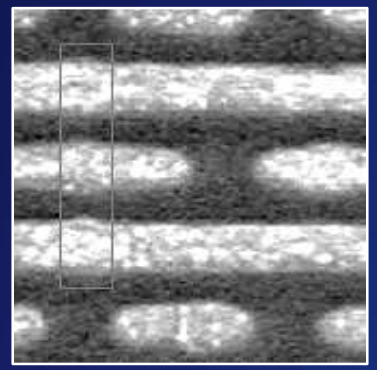
>50 Years of Scaling

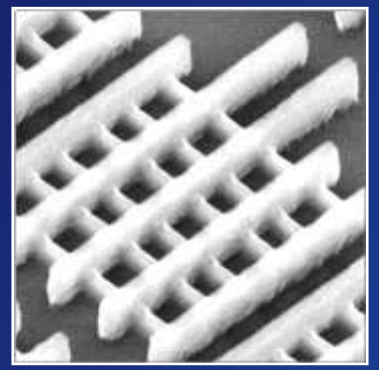


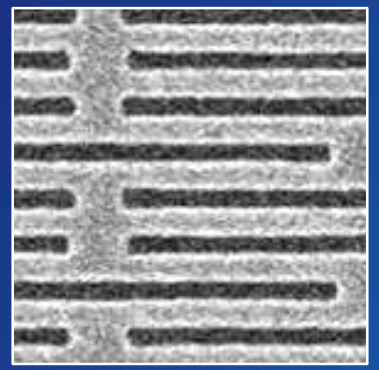
Technology Innovation

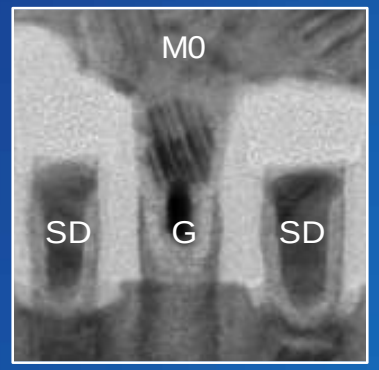










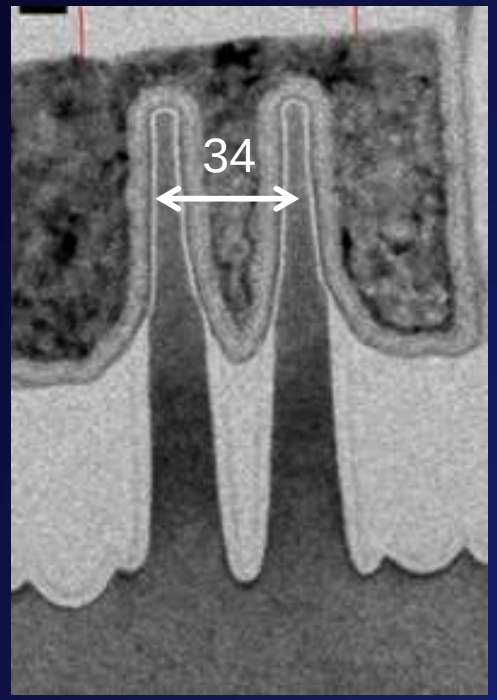


Strained Silicon	High-k Metal Gate	Self Align Via	FinFET Transistor	Hyper Scaling	Hyper Scaling
90 nm	45 nm	32 nm	22 nm	14 nm	10 nm

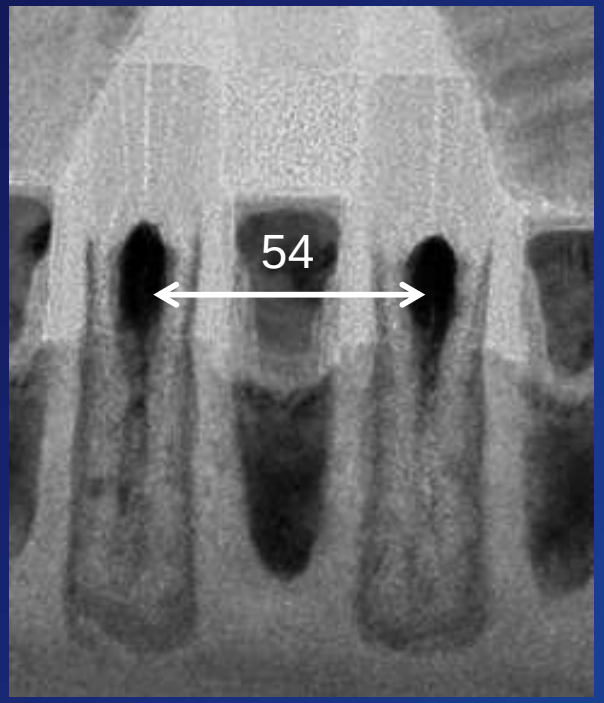
Generation

Innovations in IC Materials & Structures Continue Scaling

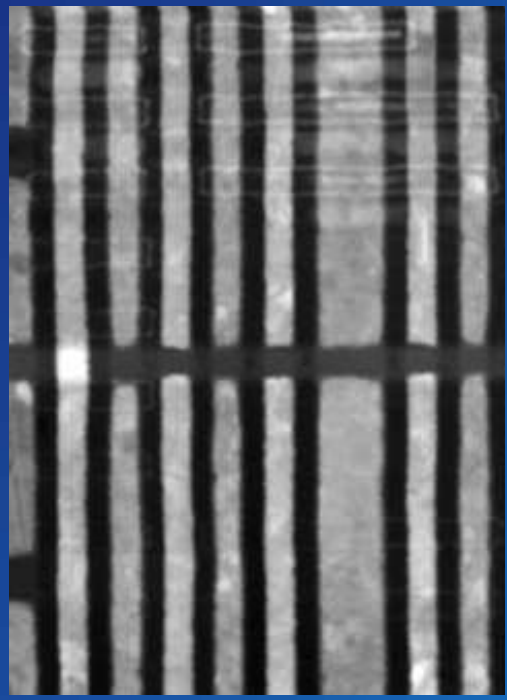
Scaled 10 nm Features



34 nm Fin Pitch



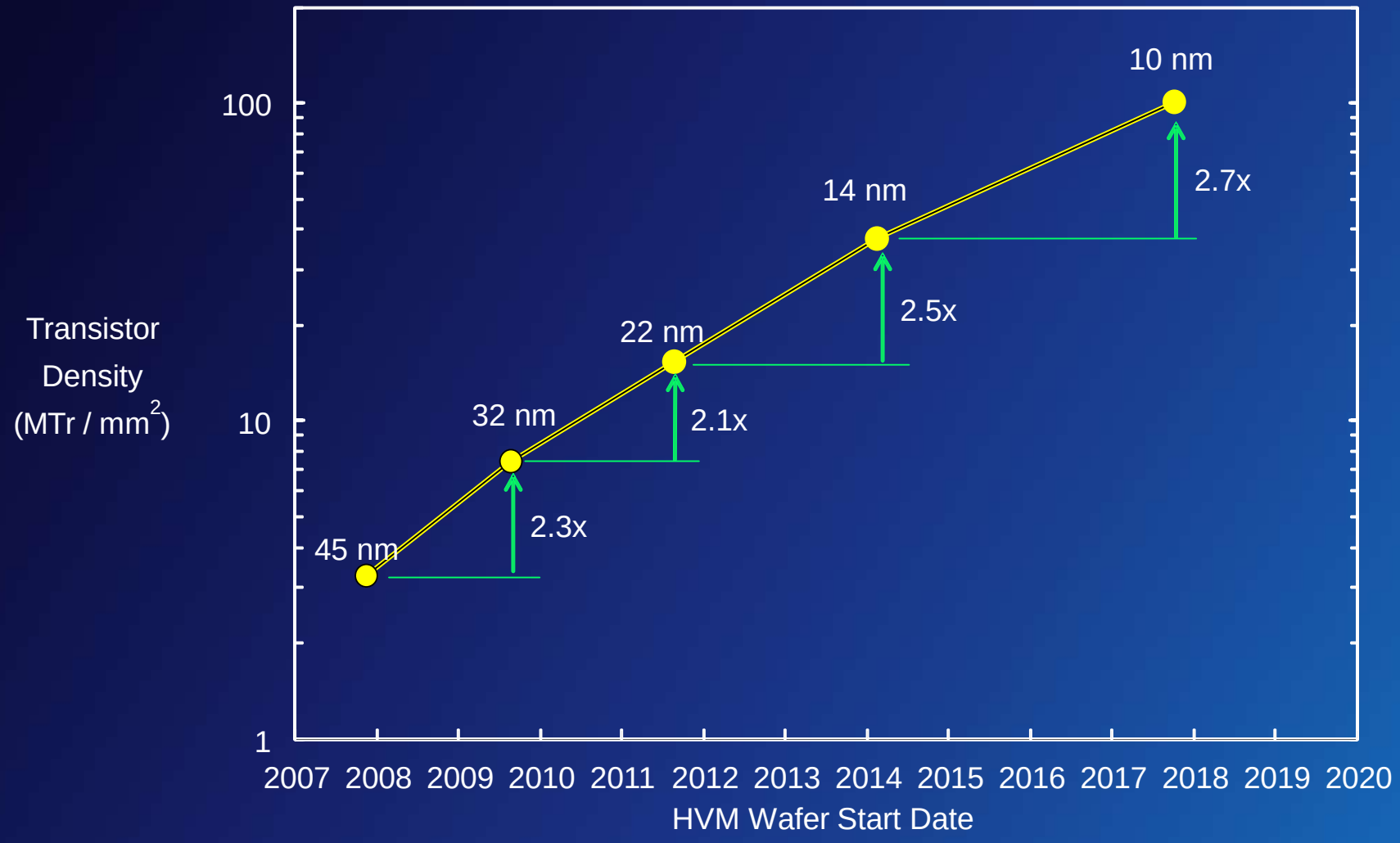
54 nm Gate Pitch



40 nm M0 Pitch
36 nm M1 Pitch
44 nm M2 Pitch

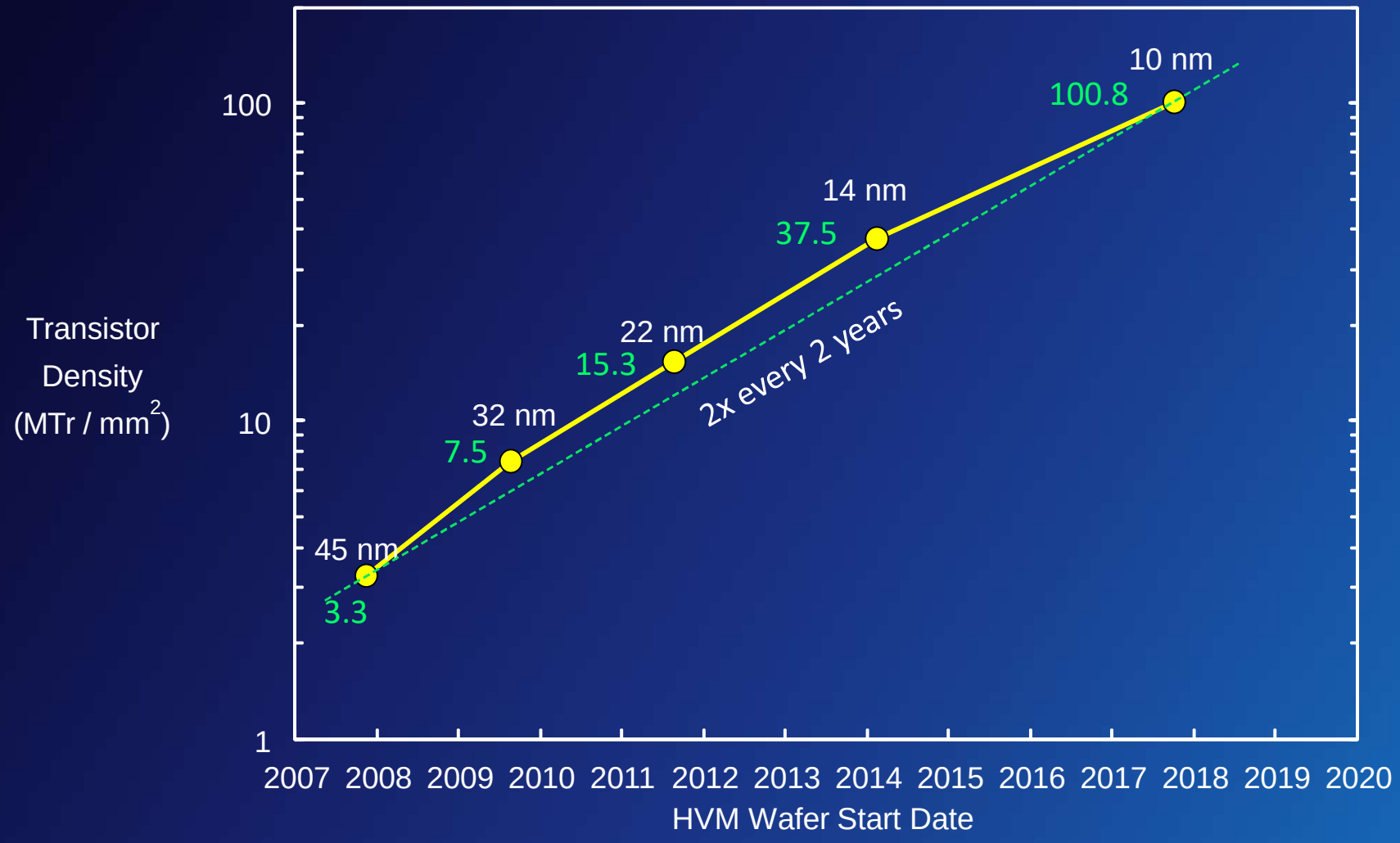
Aggressive Pitch Scaling Improves Density

Logic Transistor Density Trend



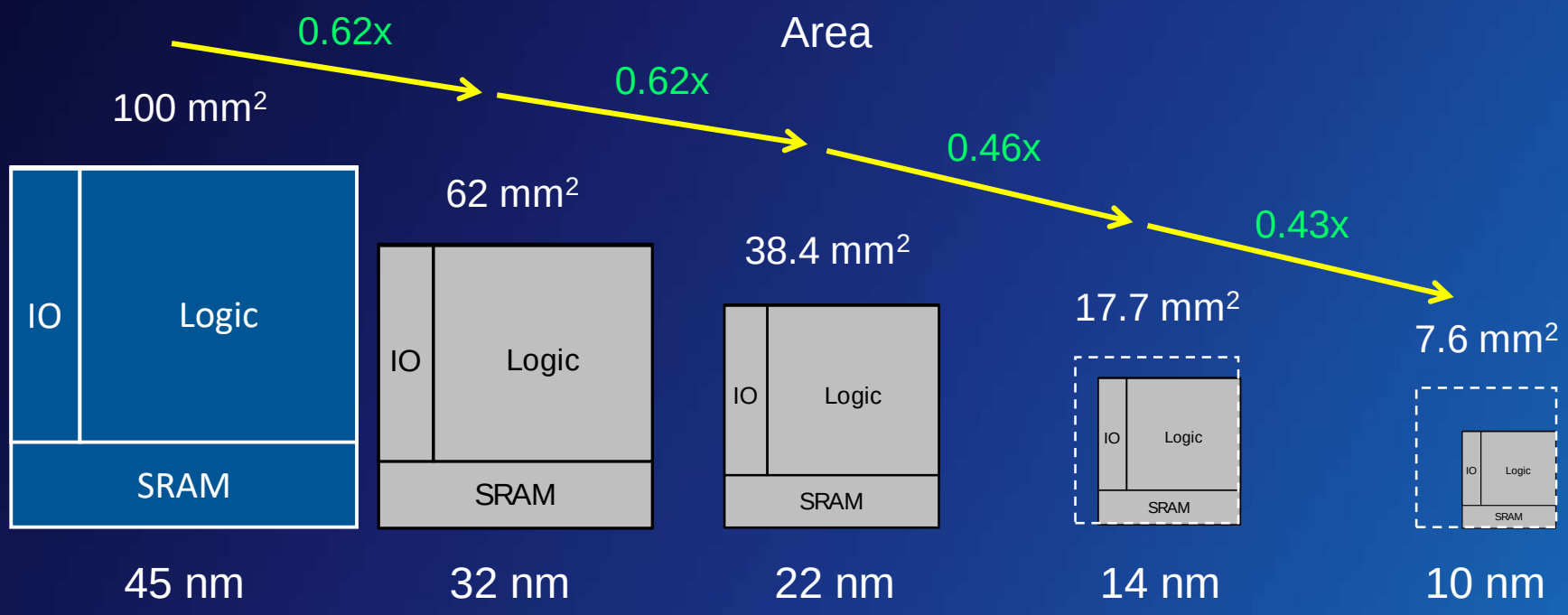
Hyper Scaling Unprecedented 2.5-2.7x Transistor Density

Logic Transistor Density Trend



Transistor Density Continues ~Doubling Every 2 Years

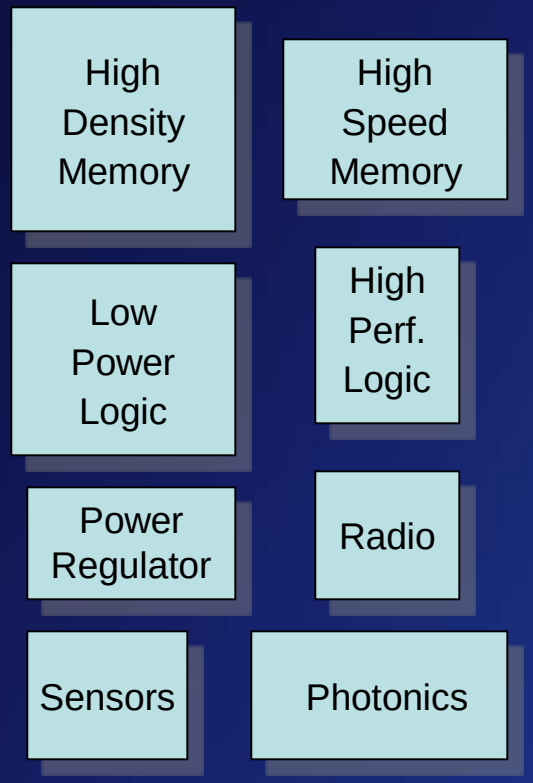
Microprocessor Die Area Scaling



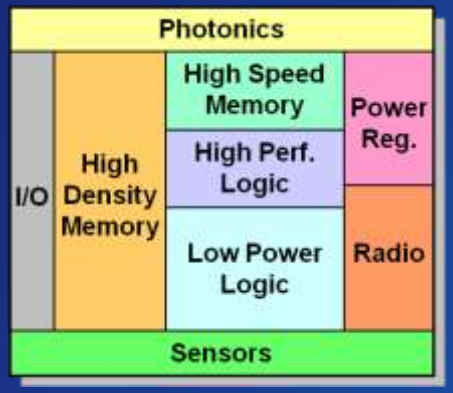
Hyper Scaling 0.46-0.43x die area scaling on 14nm & 10nm

Heterogeneous System Integration

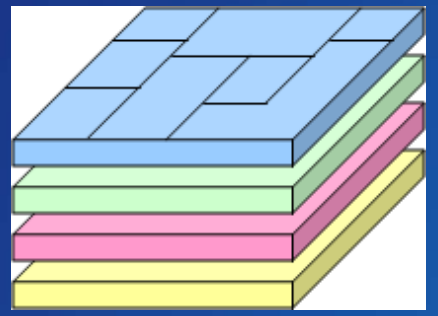
Discrete ICs



2-D Integration (SoC)

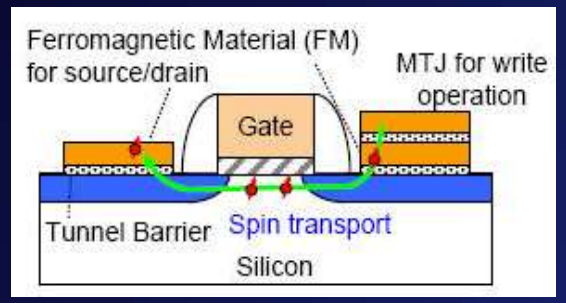


3-D Integration (SiP)

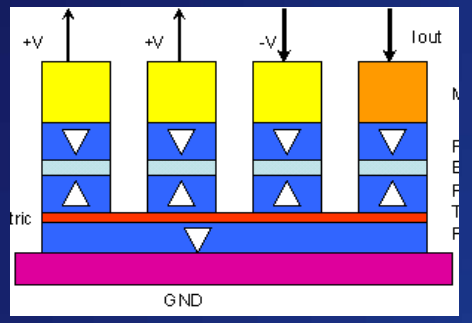


Logic
Memory
Power Reg.
Radio
Sensors
Photonics

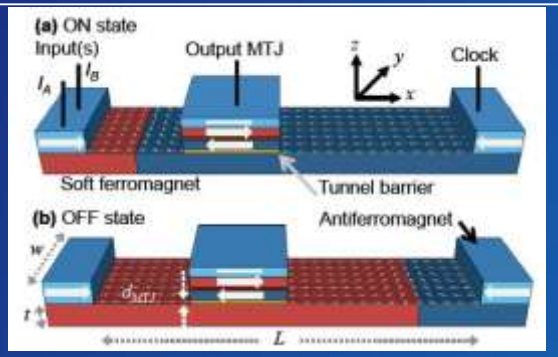
Beyond CMOS Devices - Spintronic



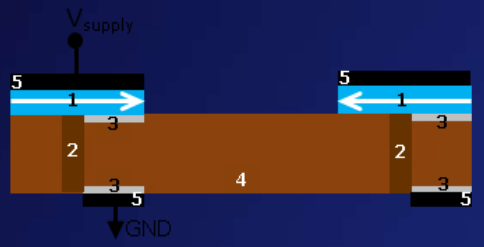
SpinFET



Spin Torque Majority Gate (SMG)

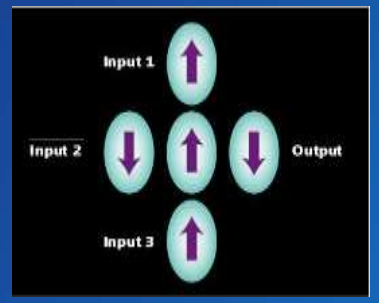


Spin Torque Domain Wall (STT/DW)

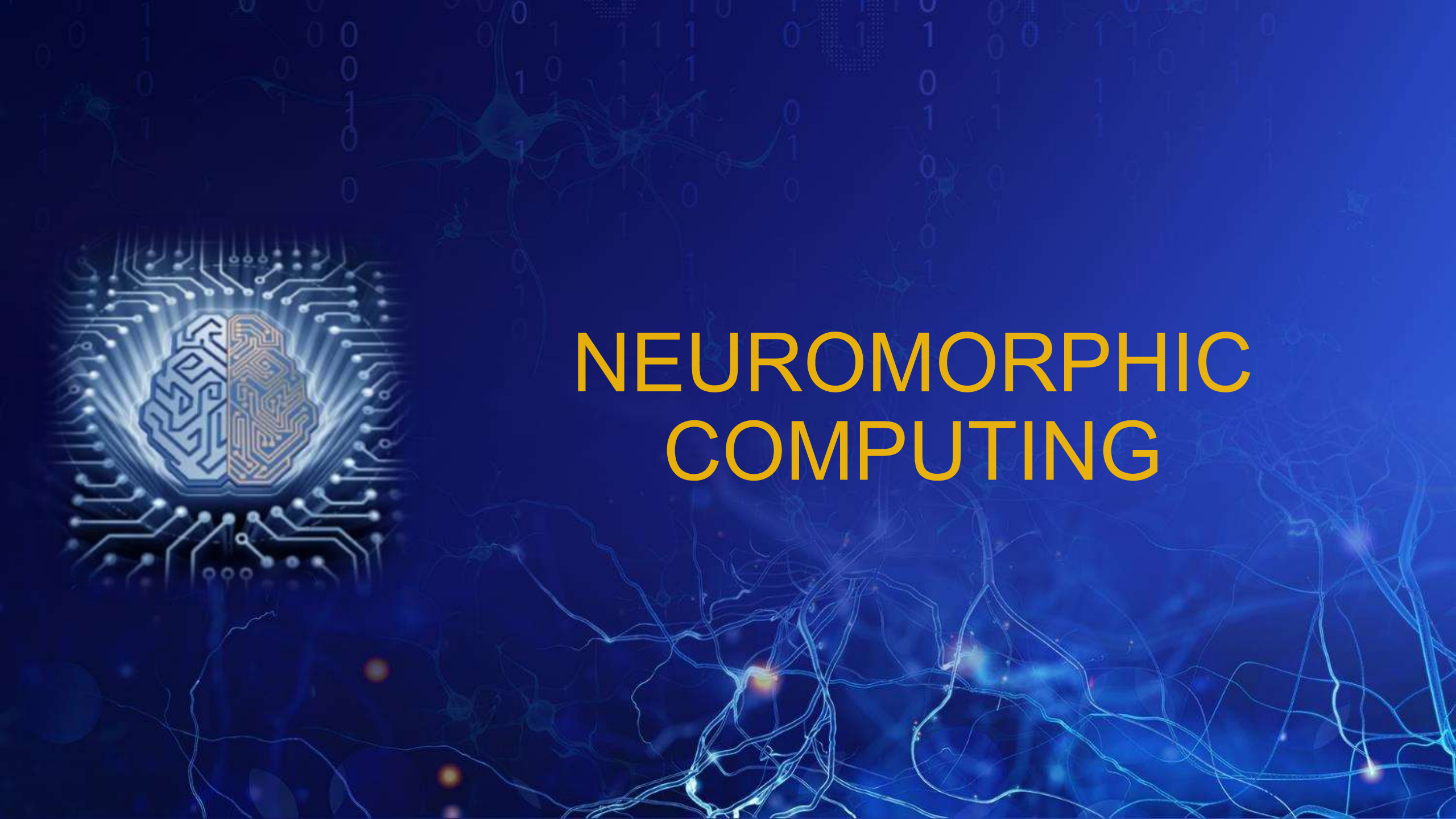


All Spin Logic (ASL)

Spin Wave Device (SWD)



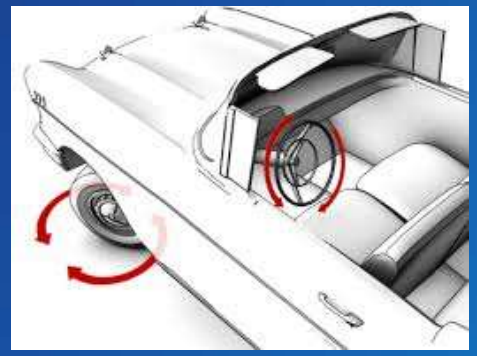
Nanomagnetic Logic (NML)


NEUROMORPHIC
COMPUTING

Modes of Event-Driven Learning

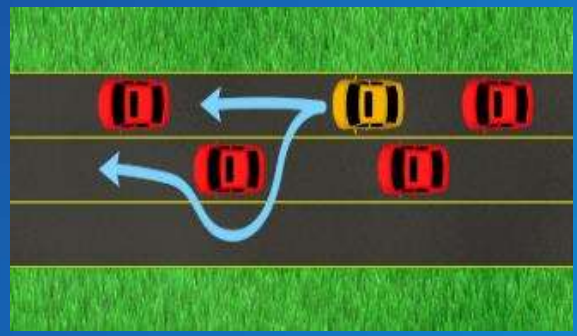
Unsupervised Learning
Pattern Detection

Self-supervised Learning
Pattern Association

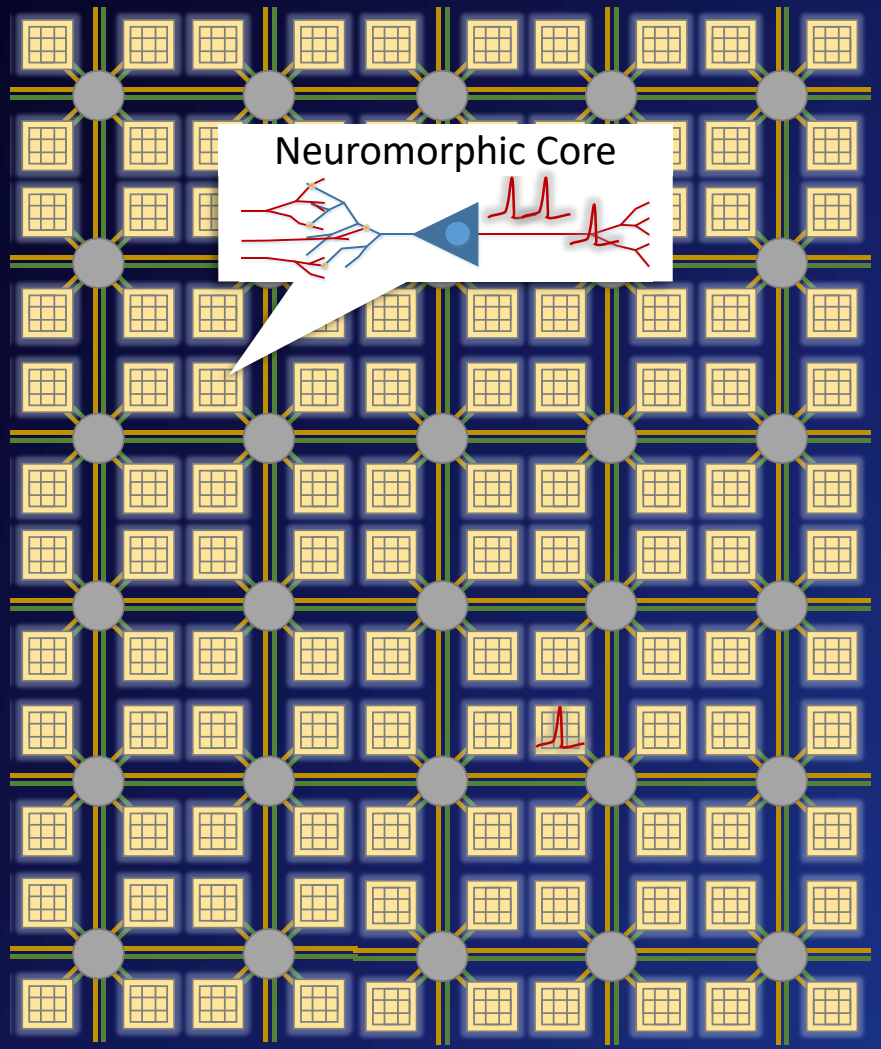


Supervised Learning
Pattern Recognition

Reinforcement Learning
Decision Making



Loihi: a Groundbreaking Research Test Chip



- Complex & unique feature set
  - Most advanced features of all published chips to date
  - 128 cores + three Lakemont cores
  - Programmable learning rules
  - Scalable neuromorphic fabric
- Novel design methodology
  - Architecture-to-silicon modeling
  - Asynchronous design flow
  - Validation of POC algorithms with FPGA-based emulation

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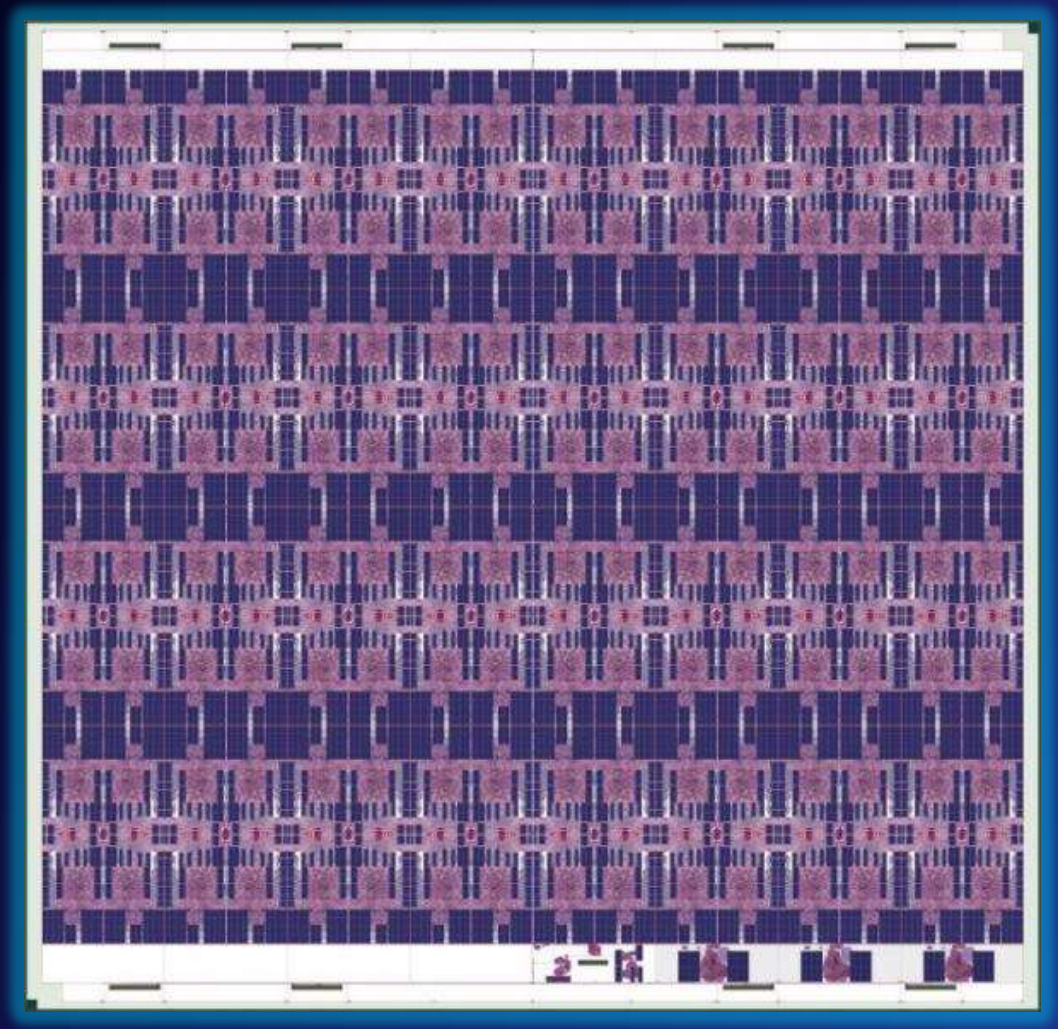

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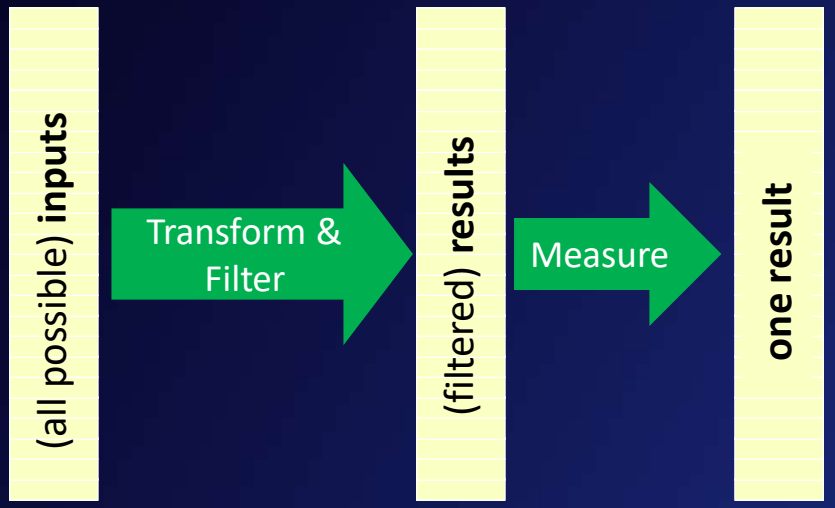
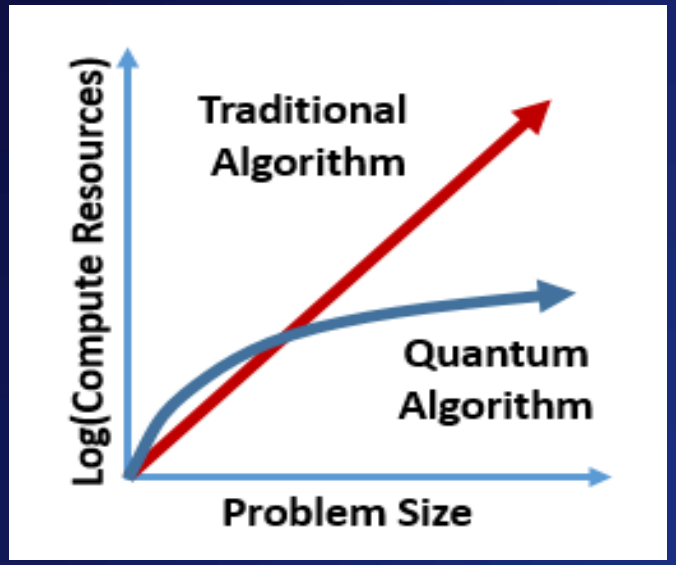
QUANTUM COMPUTING

The massive parallelism enables algorithms to tackle problems intractable for classical computers

Applications Space: HPC





~50+ Qubits: Proof of concept

- Computational power exceeds supercomputers
- Learning test bed for quantum "system"

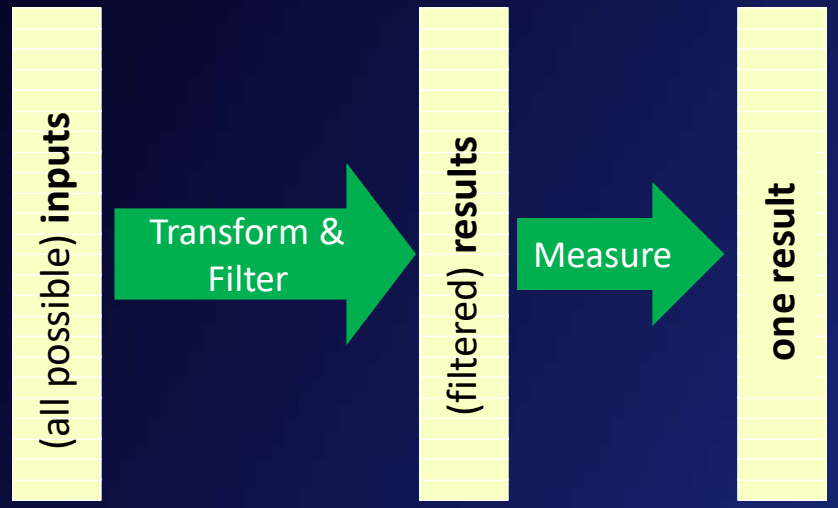
~1000+ Qubits: Small problems

- Limited error correction
- Chemistry, materials design
- Optimization

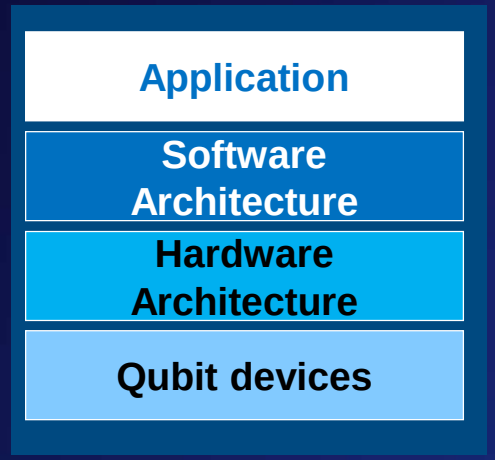
~1M+ Qubits: Commercial scale

- Fault tolerant operation
- Cryptography
- Machine Learning

Applications Space: HPC



A Quantum Computer



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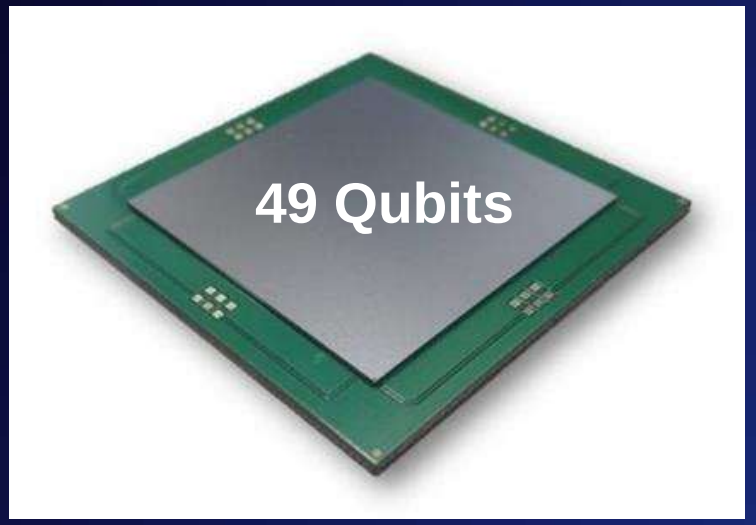
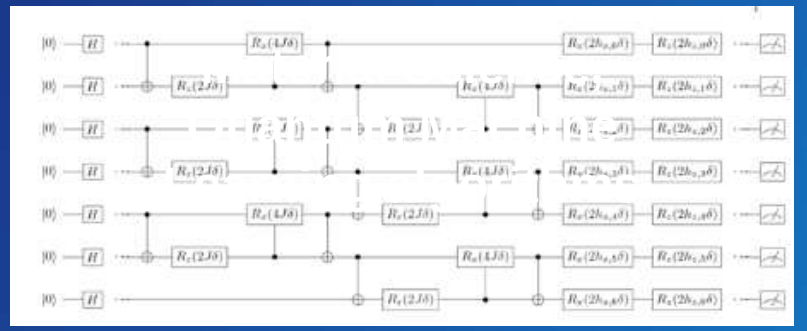
Larger Superconducting Qubit Chips



Silicon Qubits From 300mm Wafers

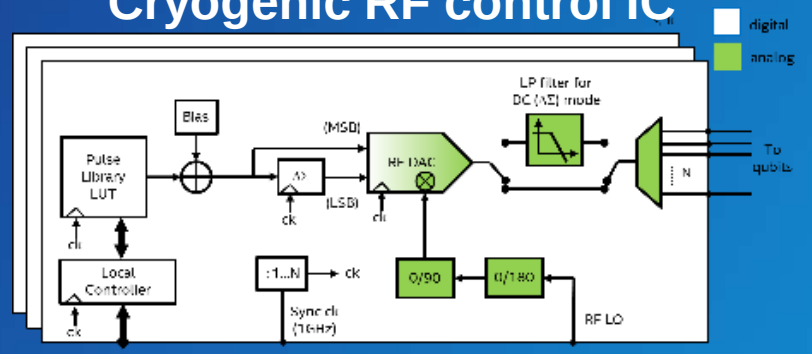
Qubit Wafer In Process

More Integrated Quantum System

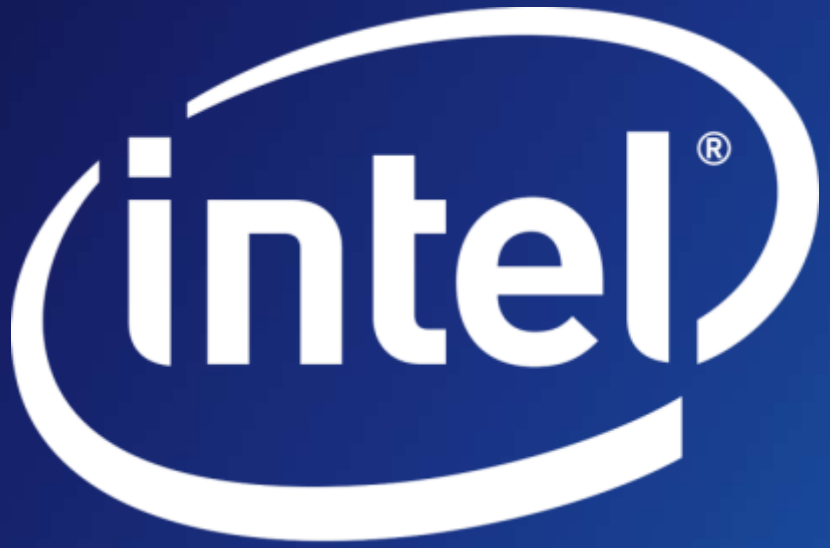


Control System Performance Simulation

Cryogenic RF control IC




The future is bright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