LEADING THE EVOLUTION OF COMPUTE

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INTEL’S RESEARCH EFFORTS

COMPONENTS RESEARCH

ENABLING MOORE’S LAW
DEVELOPING NOVEL INTEGRATION

INTEL LABS

ENABLING FUTURE PRODUCT CAPABILITIES
ANTICIPATING FUTURE INTEL

UNIVERSITY RESEARCH

Expanding the Frontier, Future Intel Collaborators
“The number of transistors and resistors on a chip doubles every 24 months”

-Gordon Moore
>50 Years of Scaling
Technology Innovation

Strained Silicon
90 nm

High-k Metal Gate
45 nm

Self Align Via
32 nm

FinFET Transistor
22 nm

Hyper Scaling
14 nm

Hyper Scaling
10 nm

Innovations in IC Materials & Structures Continue Scaling
Scaled 10 nm Features

34 nm Fin Pitch

54 nm Gate Pitch

40 nm M0 Pitch
36 nm M1 Pitch
44 nm M2 Pitch

Aggressive Pitch Scaling Improves Density
Logic Transistor Density Trend

Transistor Density (MTr/mm²)

HVM Wafer Start Date

Hyper Scaling Unprecedented 2.5-2.7x Transistor Density
Transistor Density Continues ~Doubling Every 2 Years
Microprocessor Die Area Scaling

Hyper Scaling 0.46-0.43x die area scaling on 14nm & 10nm
Heterogeneous System Integration

Discrete ICs
- High Density Memory
- Low Power Logic
- Power Regulator
- Sensors
- Photonics

High Speed Memory
- High Perf. Logic
- Radio

2-D Integration (SoC)
- I/O
- High Density Memory
- High Speed Memory
- High Perf. Logic
- Low Power Logic
- Radio
- Sensors
- Photonics

3-D Integration (SiP)
- Logic
- Memory
- Power Reg.
- Radio
- Sensors
- Photonics
## Beyond CMOS Devices - Spintronic

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Image</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SpinFET</td>
<td><img src="image" alt="SpinFET Diagram" /></td>
<td>Ferromagnetic material (FM) for source/drain, MTJ for write operation</td>
</tr>
<tr>
<td>Spin Torque Majority Gate</td>
<td><img src="image" alt="Spin Torque Majority Gate Diagram" /></td>
<td>ON state input(s), output MTJ, Clock</td>
</tr>
<tr>
<td>Nanomagnetic Logic (NML)</td>
<td><img src="image" alt="NML Diagram" /></td>
<td>Spin Wave Device, Input 1, Input 2, Input 3, Output</td>
</tr>
<tr>
<td>All Spin Logic (ASL)</td>
<td><img src="image" alt="ASL Diagram" /></td>
<td>magnetization change, spin wave bus, quartz substrate</td>
</tr>
<tr>
<td>Spin Torque Domain Wall (STT/DW)</td>
<td><img src="image" alt="STT/DW Diagram" /></td>
<td>Soft ferromagnet, tunnel barrier, antiferromagnet, output MTJ, Clock</td>
</tr>
<tr>
<td>Spin Wave Device (SWD)</td>
<td><img src="image" alt="SWD Diagram" /></td>
<td>Spin wave bus, quartz substrate</td>
</tr>
</tbody>
</table>

**SpinFET**
- Ferromagnetic material (FM) for source/drain
- MTJ for write operation

**Spin Torque Majority Gate (SMG)**
- ON state input(s)
- Output MTJ
- Clock

**Spin Torque Domain Wall (STT/DW)**
- Soft ferromagnet
- Tunnel barrier
- Antiferromagnet
- Output MTJ
- Clock
NEUROMORPHIC COMPUTING
Modes of Event-Driven Learning

Unsupervised Learning
Pattern Detection

Self-supervised Learning
Pattern Association

Supervised Learning
Pattern Recognition

Reinforcement Learning
Decision Making
Loihi: a Groundbreaking Research Test Chip

- Complex & unique feature set
  - Most advanced features of all published chips to date
  - 128 cores + three Lakemont cores
  - Programmable learning rules
  - Scalable neuromorphic fabric

- Novel design methodology
  - Architecture-to-silicon modeling
  - Asynchronous design flow
  - Validation of POC algorithms with FPGA-based emulation
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QUANTUM COMPUTING

The massive parallelism enables algorithms to tackle problems intractable for classical computers.
Applications Space: HPC

~50+ Qubits: Proof of concept
  • Computational power exceeds supercomputers
  • Learning test bed for quantum “system”

~1000+ Qubits: Small problems
  • Limited error correction
  • Chemistry, materials design
  • Optimization

~1M+ Qubits: Commercial scale
  • Fault tolerant operation
  • Cryptography
  • Machine Learning

(all possible) inputs
Transform & Filter
(filtered) results
Measure
one result
Applications Space: HPC

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- Machine Learning
Larger Superconducting Qubit Chips

Silicon Qubits From 300mm Wafers

More Integrated Quantum System

17 Qubits

49 Qubits

Qubit Wafer In Process

Control System Performance Simulation

Cryogenic RF control IC
The future is bright
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