



“What will Intel be working on in 2015?”

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Director of Marketing

**Technical Computing Group**

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# Hopefully, enabling your discoveries...

### Case Study: Building a 3D Model of the Milky Way Galaxy using 2D Sky Surveys

**Goal:** Build a 3D model of the Milky Way Galaxy using a large volume of 2D data from the surveys.

**Method:** Bayesian inference. Model the Galaxy, derive the 3D data, infer 3D model parameters, show & repeat.

**Challenges:** modeling the process of starbirth; handling of cosmic dust by sunlight; to each pixel of a 40 gig. is very hard computing. With an optimized code, **Intel Xeon Phi** saves the cost.



## REAL SCIENCE USING STAMPEDE'S XEON PHI

Romana Antoni and Jacob Durant answer questions on modeling of the flu virus

Published on December 15, 2014 by Intel Inside

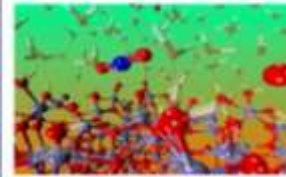


## PNNL Shifts Computational Chemistry into Overdrive

By Intel Inside

For Intel Inside, PNNL, and Molecular Dynamics, LLC

Get this information on high performance computing, performance, data storage solutions and more at [Intel Inside](#)



Our computational chemists are an impatient lot.

Despite the fact that we routinely deal with highly complicated chemical processes running on our laboratory's equally complex high performance computing (HPC) clusters, we want answers in minutes or hours, not days, months or even years.

June 30, 2014

### Mizuho Securities Delights Its Clients with Help from Intel Xeon Phi

**Now Xeon Phi-based system delivers a 30-fold speed up in calculation time**

"Strating.jp" will be clients in the form of outstanding financial returns, is one of the stated goals of Mizuho Securities Co. The institution is a member of the Mizuho Financial Group, one of Japan's three major megabanks.

Akihiro Nakajima, President and CEO of Mizuho Securities, in his announcement last year of the company's Medium-Term Business Plan, indicated that increasing the company's overall capabilities is a key part of realizing this objective. And that includes enhancing its industry-leading financial technology -- including HPC.

In particular, the company's Credit & Derivatives Trading Department is one of the



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## Intel Xeon Phi Provides Cambridge 30x Speedup in Production COSMOS WALLS Code

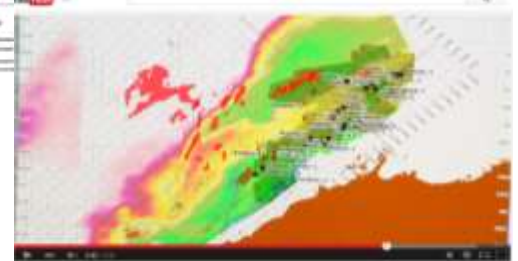
October 10, 2014 by Rob Farber - Leave a Comment

Professor Paul Shellard, the COSMOS Director at Cambridge University reports a 30x speedup of the heavily utilized production WALLS code and he notes "Our expectation is that all our cosmological field theory codes like HILLS will have similarly large speedups when optimized and ported to Xeon Phi." Currently the project is transferring a larger portion of the CMB analysis to Intel Xeon Phi coprocessors over the next twelve months.

### Center for Theoretical Physics

#### QC: Quantum Chromodynamics

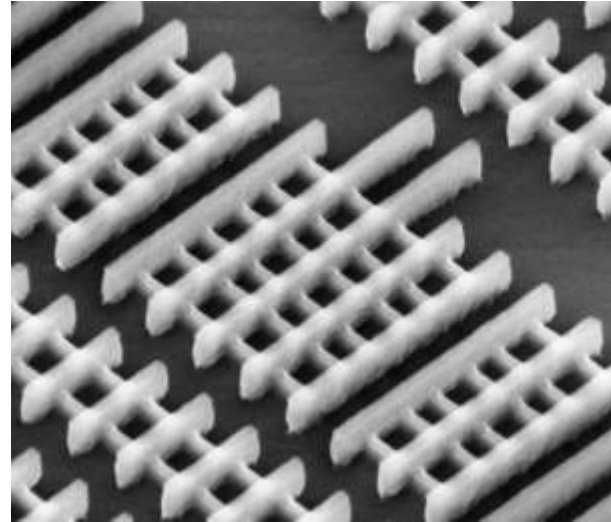
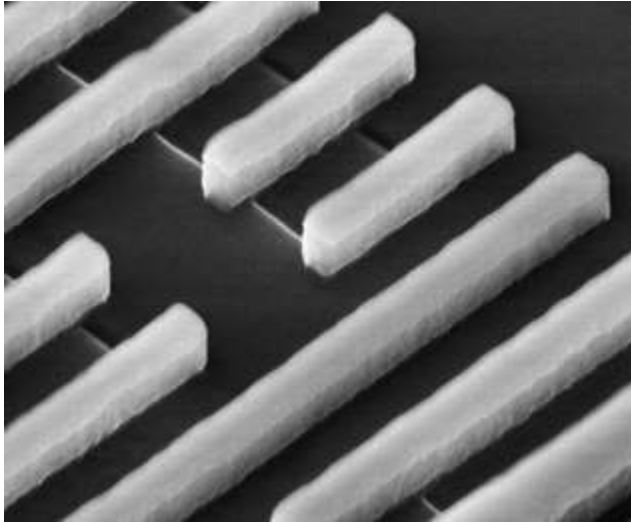
Understanding the structure of hadrons is one of the great unsolved problems in physics, and all right in the subject of high energy physics and cosmology after all. While this gets the mathematical treatment in the long range of interactions, all one of the basic theory of quarks, leptons, and photons is the standard and quantum chromodynamics (QCD) is also one of the hardest in the sense that it is non-perturbative. In addition, the spin structure of the nucleon is also one of the hardest problems in physics, and this is also one of the hardest problems in physics. The spin structure of the nucleon is also one of the hardest problems in physics, and this is also one of the hardest problems in physics.



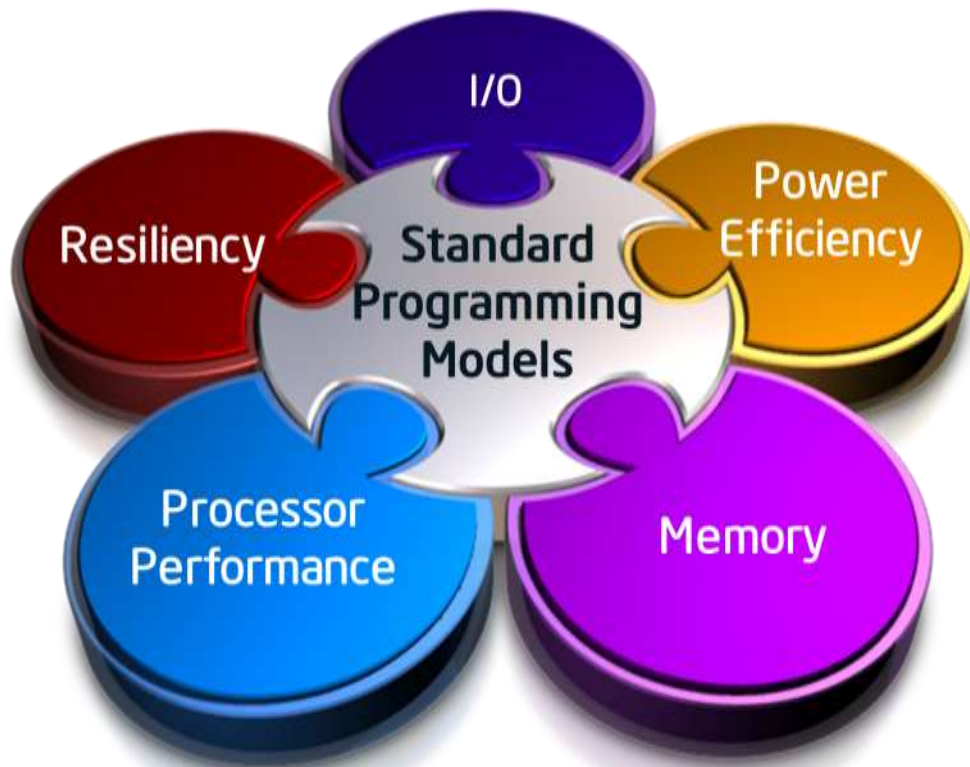
DownUnder Goes Up and Over - Leading the way in high performance



# Continuing to improve the fundamental building blocks of technology



# HPC Challenges Extend Beyond The CPU



# Two Major New Products in Development

**Knights Landing**  
Holistic Approach to Real Application Breakthroughs

**Platform Memory**  
Up to 384 GB DDR4 (6 ch)

**Compute**

- Intel® Xeon® Processor Binary-Compatible
- 3+ TFLOPS<sup>1</sup>, 3X ST<sup>2</sup> (single-thread)
- 2D Mesh Architecture
- Out-of-Order Cores

**On-Package Memory**

- Over 5X STREAM vs. DDR4<sup>3</sup>
- Up to 16 GB at launch

**Omni-Path (optional)** • 1<sup>st</sup> Intel processor to integrate

**I/O** Up to 36 PCIe 3.0 lanes

Optimize and validate your performance. You may have better options for performance, only on Intel microprocessors.  
Performance based on STREAM using specific compiler, system, containers, software, operations, and functions. Any change to any of those factors may cause the results to vary. You should consult the literature and performance tests to better understand real-world, user customized, scenarios, including the performance of the product, what controls you use, other products.  
For more complete information, visit [intel.com/acceleration](http://intel.com/acceleration). © 2015 Intel Corporation.

Coming 2H'15

Intel® Omni-Path Architecture—Makes it even Better  
Benefits for "Every" Scale. Brings disruptive economics to the fabrics market

**1 Better System Scaling**  
48 port Switch Chip Architecture  
vs. 48 in 100 in Bond

**2 Better Application Scaling**  
100 Gbps Line speed

56% Lower Latency<sup>4</sup>

**Small Clusters**  
Higher Port Density  
48 ports supports up to 12 dual nodes by only adding CABLES<sup>5</sup>

**Mainstream Clusters**  
Fewer Switches<sup>2</sup>

**Supercomputers**  
Higher Scaling  
Over 27X NODES in a 2-tier 2-hop FABRIC<sup>7</sup>

**1.3x** up to **1/2** **2.3x**

Maximize SINGLE SWITCH investment

1. As compared to a common 24-port high-end switch, a 48-port switch can support a 20% higher node density. 2. Switches are connected in a 2-tier 2-hop fabric. 3. Based on Intel's 100 Gbps Ethernet switch. 4. Latency is measured in microseconds. 5. This is based on a 48-port switch. 6. This is based on a 48-port switch. 7. This is based on a 48-port switch. © 2015 Intel Corporation.



THETA

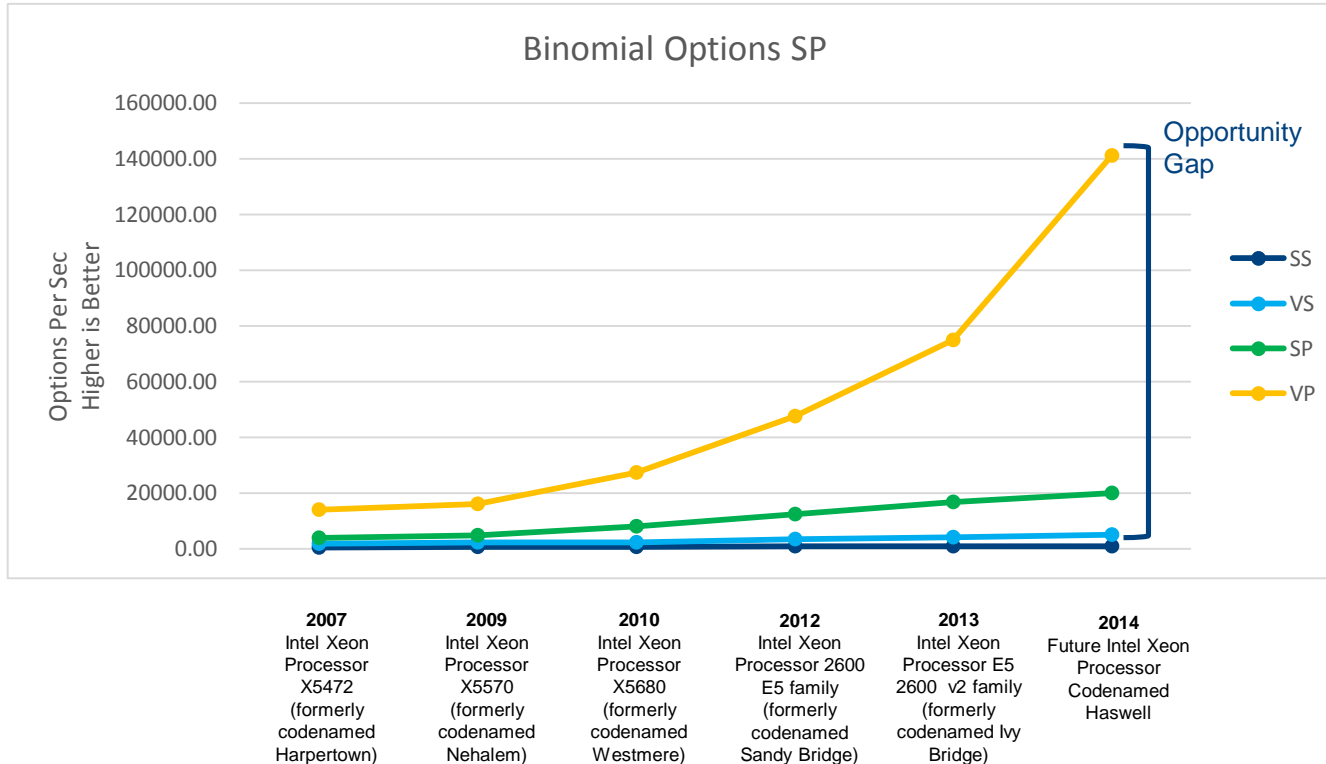


<https://software.intel.com/en-us/articles/intel-xeon-phi-coprocessor-applications-and-solutions-catalog>

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# The Power Performance Opportunity Lies in the Software



SS: Scalar and Single threaded  
 VS: Vectorized and Single threaded  
 SP: Scalar and parallel  
 VP: Vectorized and Parallelized.

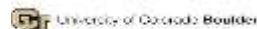
Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

Configurations: as listed on Slide 22. Performance measured in Intel Labs by Intel employees. **For more information go to**

<http://www.intel.com/performance>

fnord.

# Intel® Parallel Computing Centers Community



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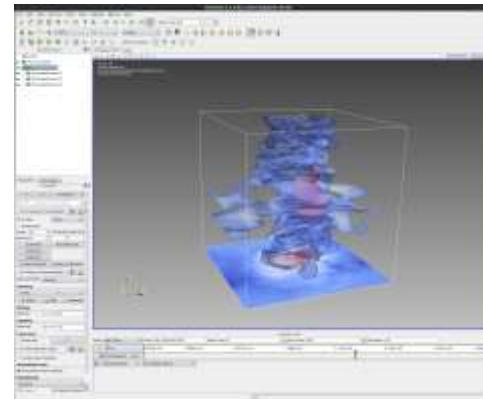
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# Contribution to Community: Software Defined Visualization

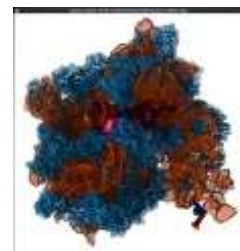


Software Visualization – Ray Trace Image on Maverick  
Model Courtesy of Florida International University\*  
Photo Courtesy of TACC\*



<http://openswr.org>

Wendell Horton Plasma Isosurface  
Rendered under Paraview using  
OpenSWR



Model Courtesy of  
Carsten Kutzner, MPI  
BPC, Goettingen.

VMD 'ribosome'  
Rendered with  
OSPRay  
Engine for High  
Fidelity Visualization

<http://ospray.org>



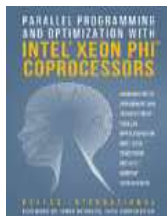
# Capturing and Transferring Knowledge



<http://www.amazon.com/Structured-Parallel-Programming-Efficient-Computation/dp/0124159931>



<http://www.amazon.com/Intel-Xeon-Coprocessor-High-Performance-Programming/dp/0124104142>



<http://www.colfax-intl.com/nd/xeonphi.aspx>



<http://click.intel.com/intel-xeon-phi/m-coprocessor-architecture-and-tools-the-guide-for-application-developers.html>



<http://store.elsevier.com/High-Performance-Parallelism-Pearls/James-Reinders/isbn-9780128021187/>

## Books, Papers, Tutorials

## Training Partners



<http://www.colfax-intl.com/nd/xeonphi/training.aspx>



<https://www.nersc.gov/users/training/events/>

## Workshops And Labs

# Some of what we're doing in '15

Continue delivering leading semiconductor processes

Collaborate to build productive, power efficient, scalable, general HPC technology

Prepare Knights Landing and Intel Omni-Path for market

Collaborate to deliver applications for the next 20 years

Thank You!

# Footnotes

All products, computer systems, dates and figures specified are preliminary based on current expectations, and are subject to change without notice.

All projections are provided for informational purposes only. Any difference in system hardware or software design or configuration may affect actual performance.

<sup>1</sup> Over 3 Teraflops of peak theoretical double-precision performance is preliminary and based on current expectations of cores, clock frequency and floating point operations per cycle.

<sup>2</sup> Projected peak theoretical single-thread performance relative to 1st Generation Intel® Xeon Phi™ Coprocessor 7120P (formerly codenamed Knights Corner)

<sup>3</sup> Projected result based on internal Intel analysis of STREAM benchmark using a Knights Landing processor with 16GB of ultra high-bandwidth versus DDR4 memory only with all channels populated.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors.

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