“What will Intel be working on in 2015?”

Joe Curley
Director of Marketing
Technical Computing Group

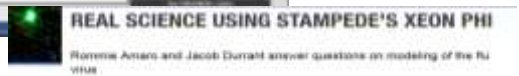
joseph.c.curley@intel.com

Hopefully, enabling your discoveries…

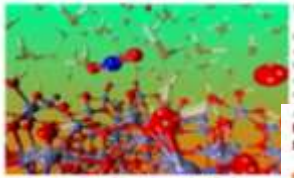
Intel Xeon Phi Provides Cambridge 30x Speedup in Production COSMOS WALLS Code

October 10, 2014 by Rob Farber — Leave a Comment

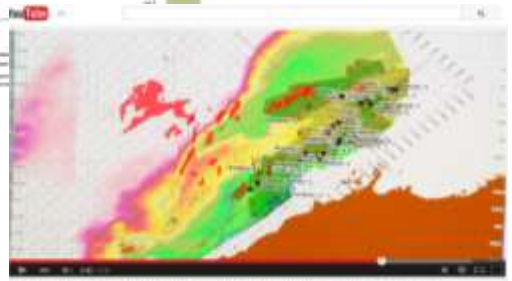
Professor Paul Shellard, the COSMOS Director at Cambridge University reports a 30x speedup of the heavily utilized production WALLS code and he notes *"Our expectation is that all our cosmological field theory codes, like WALLS, will have similarly large speed-ups when optimized and ported to Xeon Phi."* Currently the project is transferring a larger portion of the CMB analysis to Intel Xeon Phi coprocessors over the next twelve months.



PNNL Shifts Computational Chemistry into Overdrive

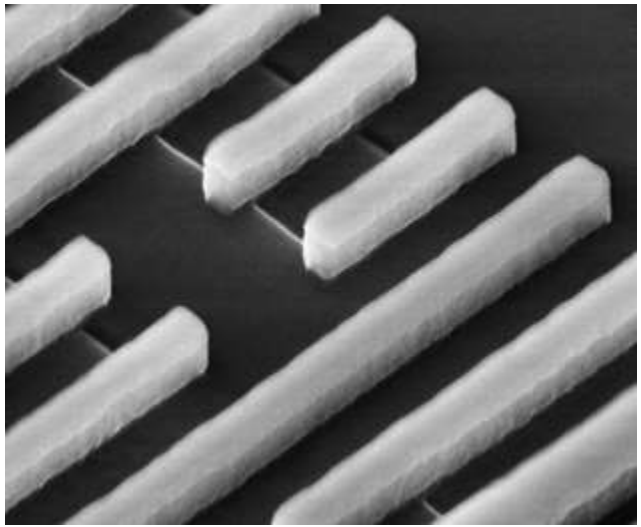


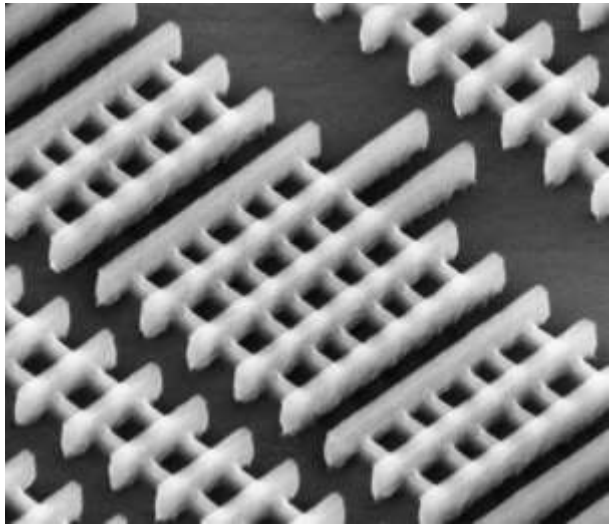
Mizuho Securities Delights Its Clients with Help from Intel Xeon Phi



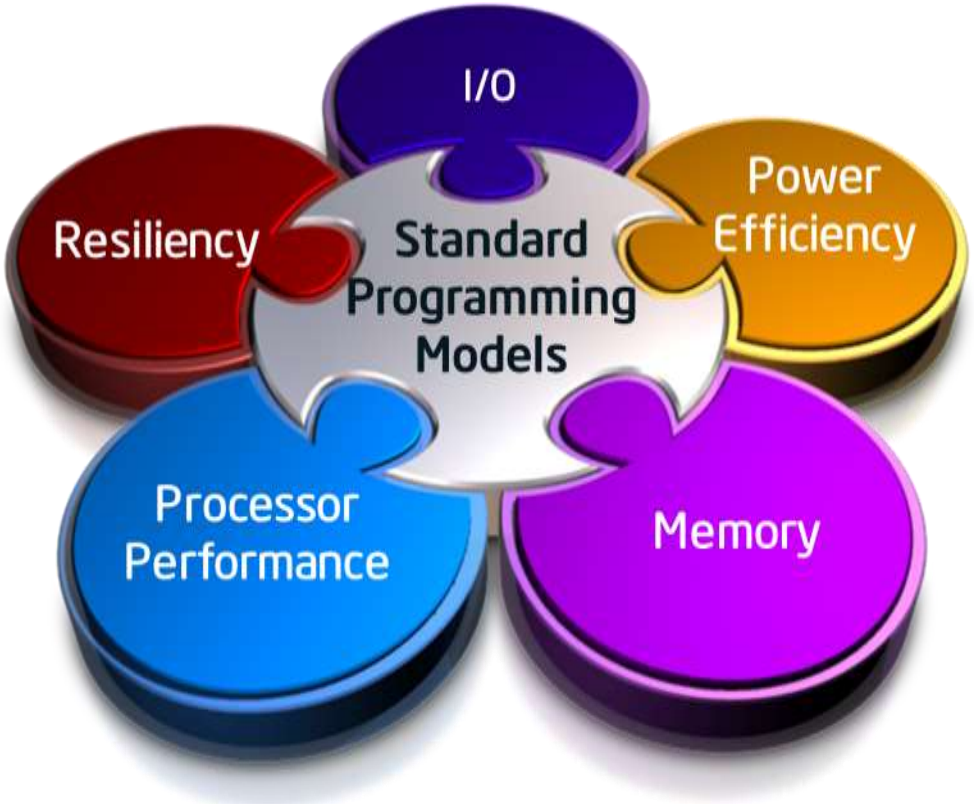
DownUnder Goes Up and Over : Leading the way in high performance

Continuing to improve the fundamental building blocks of technology

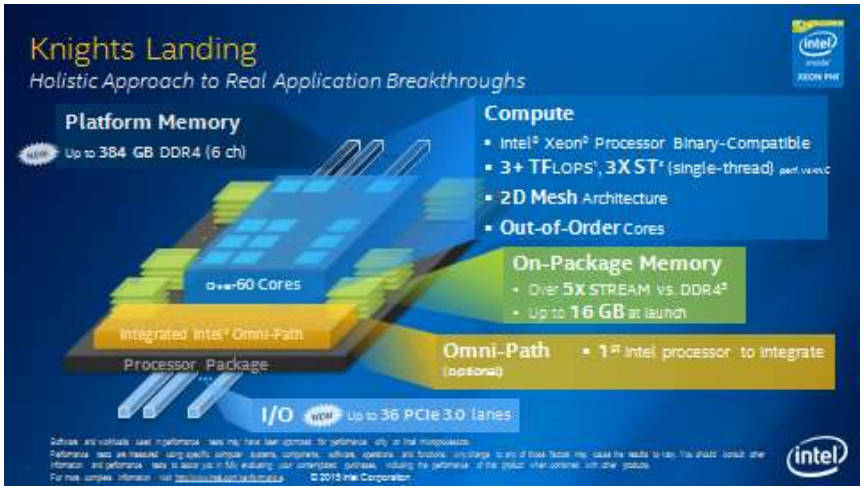


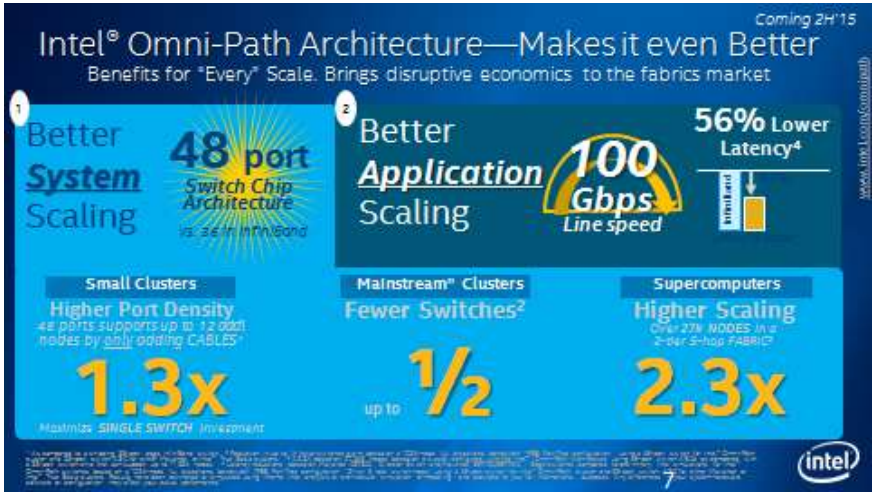


HPC Challenges Extend Beyond The CPU



Two Major New Products in Development

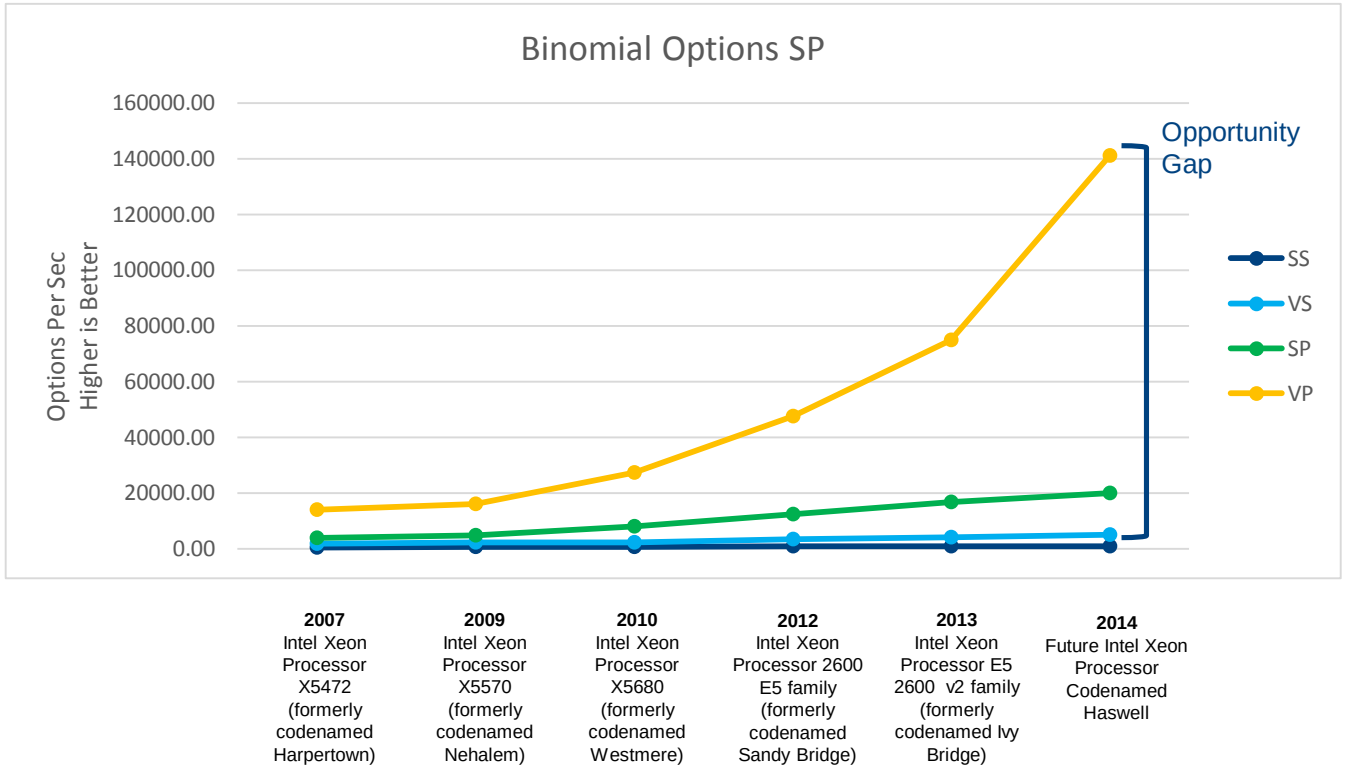




THETA

https://software.intel.com/en-us/articles/intel-xeon-phi-coprocessor-applications-and-solutions-catalog

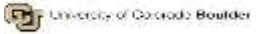
The Power Performance Opportunity Lies in the Software



SS: Scalar and Single threaded
VS: Vectorized and Single threaded
SP: Scalar and parallel
VP: Vectorized and Parallelized.

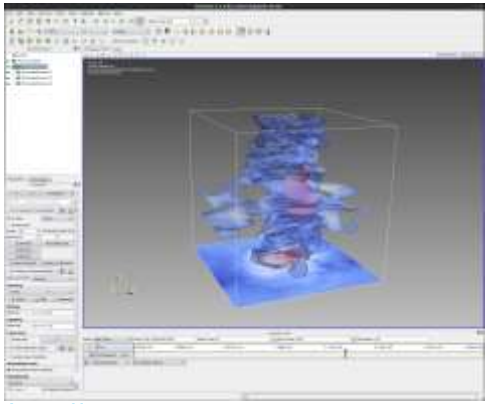
Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.
Configurations: as listed on Slide 22. Perfromance measured in Intel Labs by Intel employees. **For more information go to** http://www.intel.com/performance
fnord.

Intel® Parallel Computing Centers Community

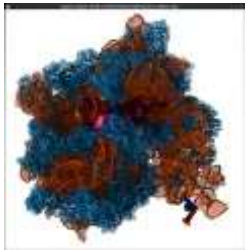


Contribution to Community: Software Defined Visualization

Software Visualization – Ray Trace Image on Maverick
Model Courtesy of Florida International University*
Photo Courtesy of TACC*



http://openswr.org
Wendell Horton Plasma Isosurface Rendered under Paraview using OpenSWR



Model Courtesy of Carsten Kutzner, MPI BPC, Goettingen.

VMD 'ribosome' Rendered with OSPRay Engine for High Fidelity Visualization

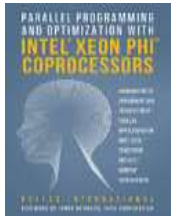
http://ospray.org

Capturing and Transferring Knowledge

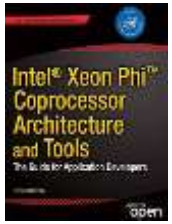
Books, Papers, Tutorials

http://www.amazon.com/Structured-Parallel-Programming-Efficient-Computation/dp/0124159931

http://www.amazon.com/Intel-Xeon-Coprocessor-High-Performance-Programming/dp/0124104142



http://www.colfax-intl.com/nd/xeonphi.aspx



http://click.intel.com/intelr-xeon-phitm-coprocessor-architecture-and-tools-the-guide-for-application-developers.html

http://store.elsevier.com/High-Performance-Parallelism-Pearls/James-Reinders/isbn-9780128021187/

Workshops And Labs

https://www.nersc.gov/users/training/events/

Training Partners

http://www.colfax-intl.com/nd/xeonphi/training.aspx

Some of what we're doing in '15

Continue delivering leading semiconductor processes

Collaborate to build productive, power efficient, scalable, general HPC technology

Prepare Knights Landing and Intel Omni-Path for market

Collaborate to deliver applications for the next 20 years

Thank You!

Footnotes

All products, computer systems, dates and figures specified are preliminary based on current expectations, and are subject to change without notice.

All projections are provided for informational purposes only. Any difference in system hardware or software design or configuration may affect actual performance.

[1] Over 3 Teraflops of peak theoretical double-precision performance is preliminary and based on current expectations of cores, clock frequency and floating point operations per cycle.

[2] Projected peak theoretical single-thread performance relative to 1st Generation Intel® Xeon Phi™ Coprocessor 7120P (formerly codenamed Knights Corner)

[3] Projected result based on internal Intel analysis of STREAM benchmark using a Knights Landing processor with 16GB of ultra high-bandwidth versus DDR4 memory only with all channels populated.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors.